

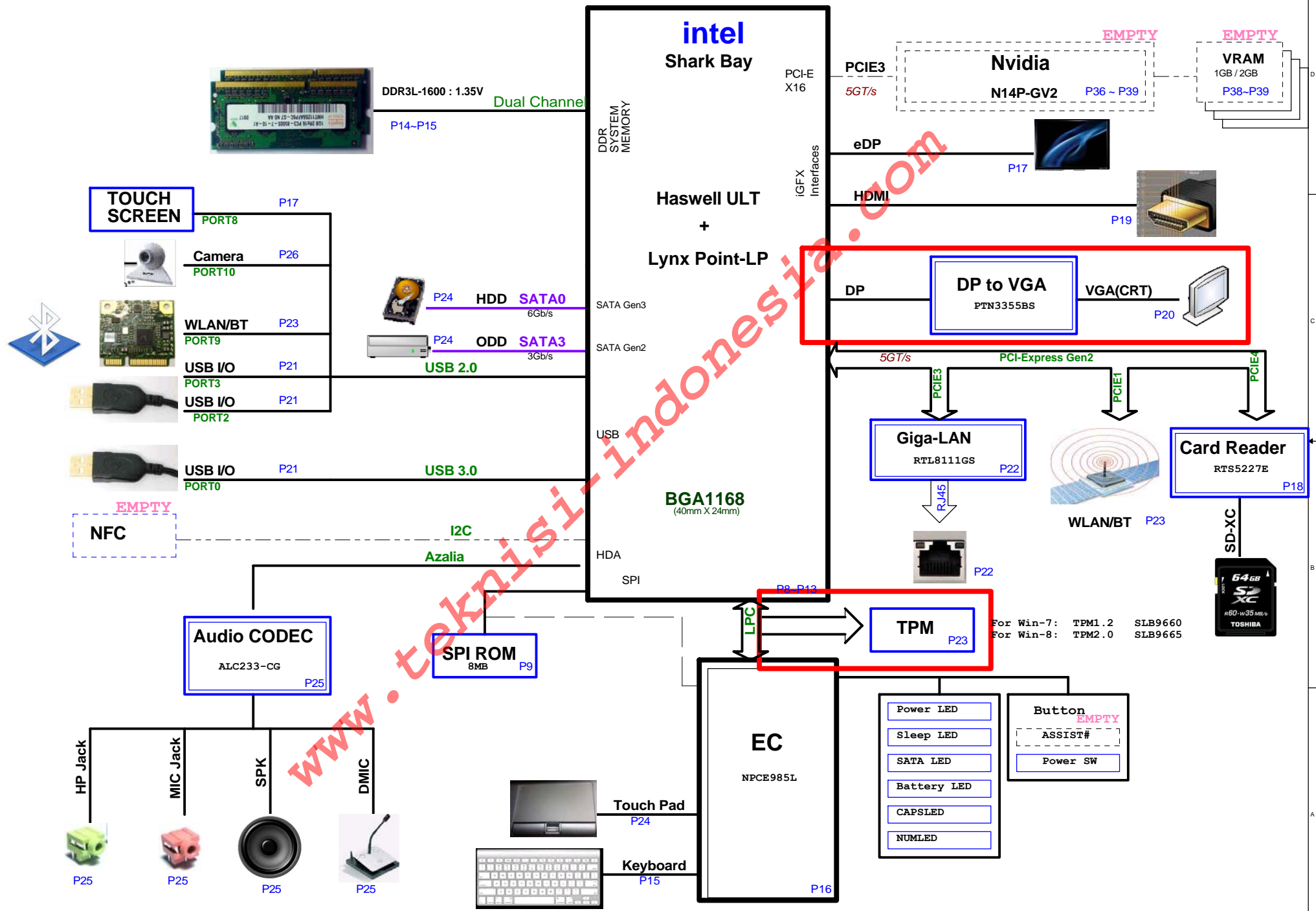
Page	Title of schematic page	Rev.	Date
01	Page List	1A	
02	Block Diagram	1A	
03	Change List	1A	
04	HSW MCP (DISPLAY/Sideband)	1A	
05	HSW MCP (MEMORY/GND)	1A	
06	HSW MCP (CFG/PwrMGT)	1A	
07	HSW MCP (POWER)	1A	
08	HSW PCH (RTC/HDA/SATA)	1A	
09	HSW PCH (PCIE/USB)	1A	
10	HSW PCH (CLK/LPC/SPI/SMB)	1A	
11	HSW PCH (GPIO/LPIO/MISC)	1A	
12	HSW PCH (POWER)	1A	
13	DDR3 DIMM0-STD (5.2H)	1A	
14	DDR3 DIMM1-RSV (5.2H)	1A	
15	HOLE/EMI/KB	1A	
16	NPCE985L & FLASH	1A	
17	LVDS/TS/NFC	1A	
18	CARD READER (RTS5227E)	1A	
19	HDMI/THERMAL	1A	
20	DP to VGA	1A	
21	USB	1A	
22	LAN (RTL8111GS)	1A	
23	WLAN/KB-BL	1A	
24	HDD/ODD/G-SENSOR/TP/FAN	1A	
25	Audio ALC233-CG	1A	
26	LED/PS/DMIC/Camera	1A	
27	POWER +VCC_CORE (NCP81101)	1A	
28	POWER 3VPCU&RVCC5 (TPS51427)	1A	
29	POWER 1.35VSUS/VTT_MEM	1A	
30	POWER +1.05V (G5602R41U)	1A	
31	POWER VCC1.5/Thermal	1A	
32	POWER (BAT IN / ADA IN/ UL)	1A	
33	POWER CHARGER (ISL88731C)	1A	
34	POWER VGA_CORE/1.0 (RT8812A)	1A	
35	POWER VCC1.5_VRAM/1.05V	1A	
36	NVIDIA N14 GB2-64 PCIE 1/4	1A	
37	NVIDIA N14 GB2-64 TMDS 2/4	1A	
38	NVIDIA N14 GB2-64 VRAM 3/4	1A	
39	NVIDIA N14 GB2-64 VRAM 4/4	1A	

Page	Title of schematic page	Rev.	Date
40	Woofers	1A	
41	IO PORT LIST	1A	
		1A	
		1A	

* : No mount
L@ : For LVDS output
D@ : For eDP output
E@ : For DIS GFX
I@ : For UMA

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HKDD Haswell ULT BLOCK DIAGRAM



Change List

MB_SCH_FVT_01
P20- DC27, DC28, DC33 change from 15p to 3.3p
Reason : Base on EVT aRGB VEVS, fine tune the value
Possible Risk: No.

MB_SCH_FVT_02
P23- Add F8 for TPM D/B
Reason : Base on EVT overload result.
Possible Risk: No.

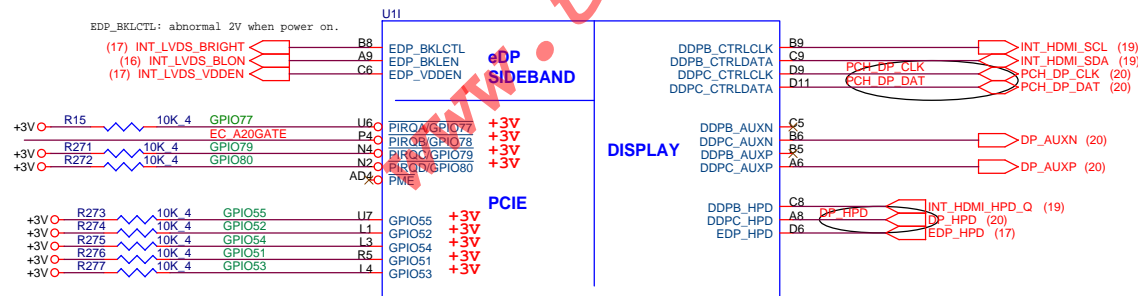
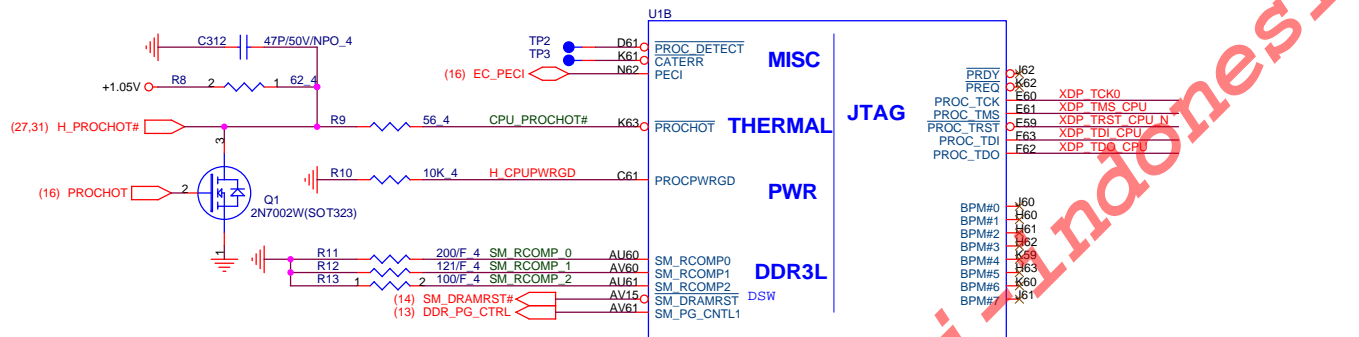
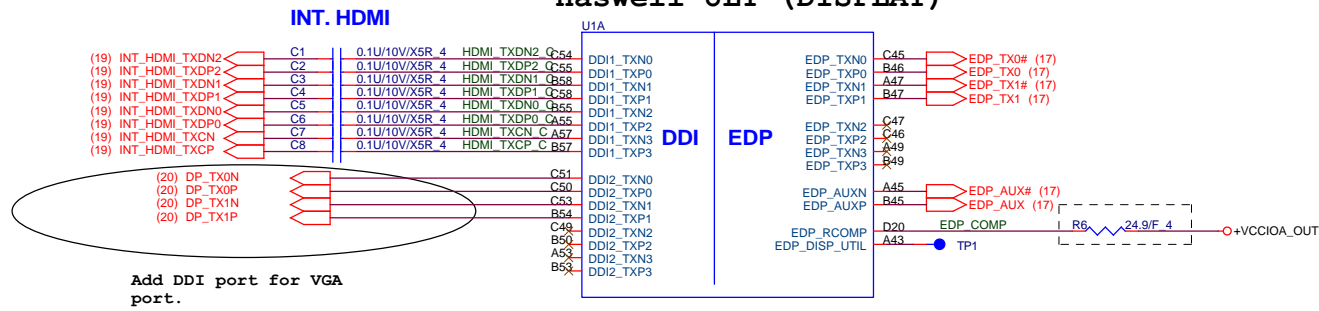
MB_SCH_FVT_03
P10- Add 33 ohm for LPC_FRAME#
Reason : the overshoot and undershoot is big, add 33 ohm to reduce
Possible Risk: No.

MB_SCH_FVT_04
P23- Add SW1 for TPM _ID select
Reason : Reserve for TPM_ID SW used
Possible Risk: No.

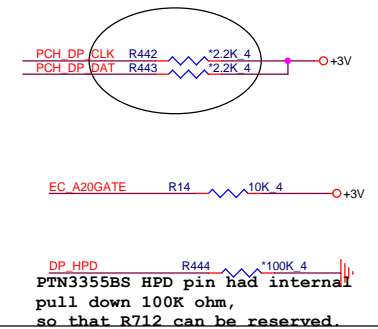
MB_SCH_EVT_05
P22- CON14, C270, F7, R239, R240, Q18, Q19, R241 change to no mount
Reason : Delete Keyboard light function for RFQ requirement
Possible Risk: No.

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Haswell ULT (DISPLAY)



Add DDI port for VGA port.



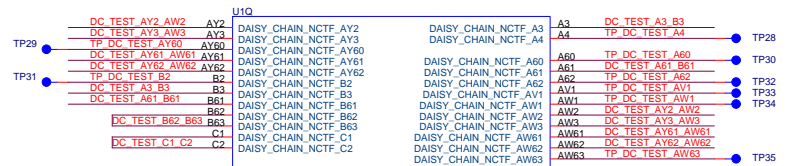
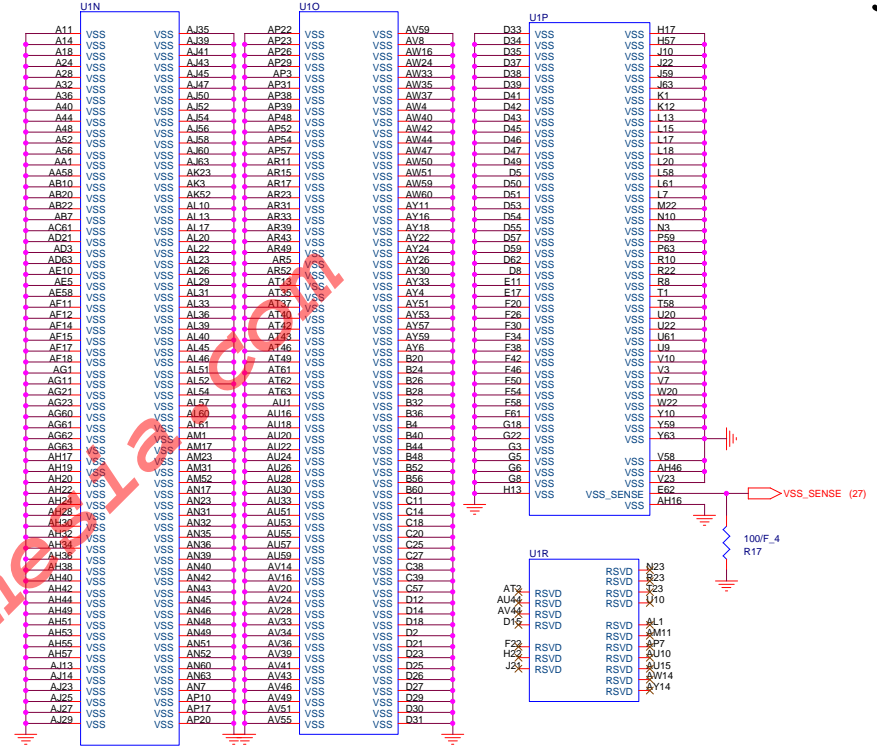
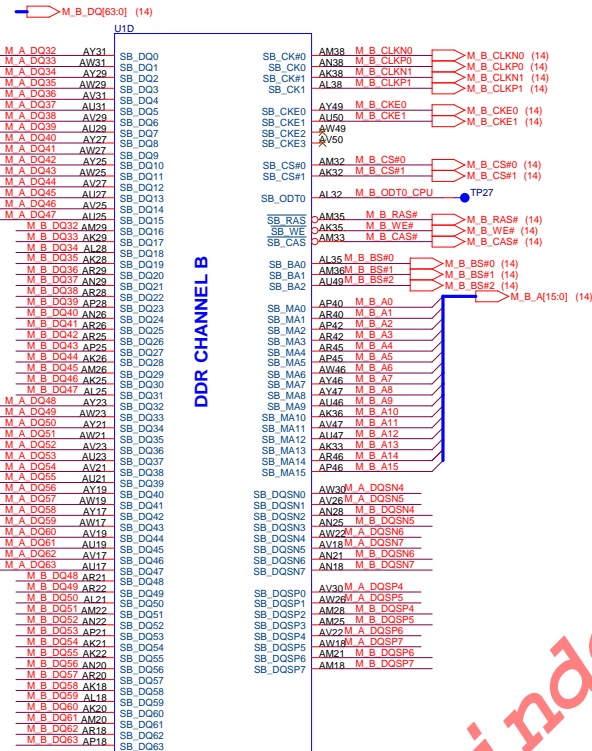
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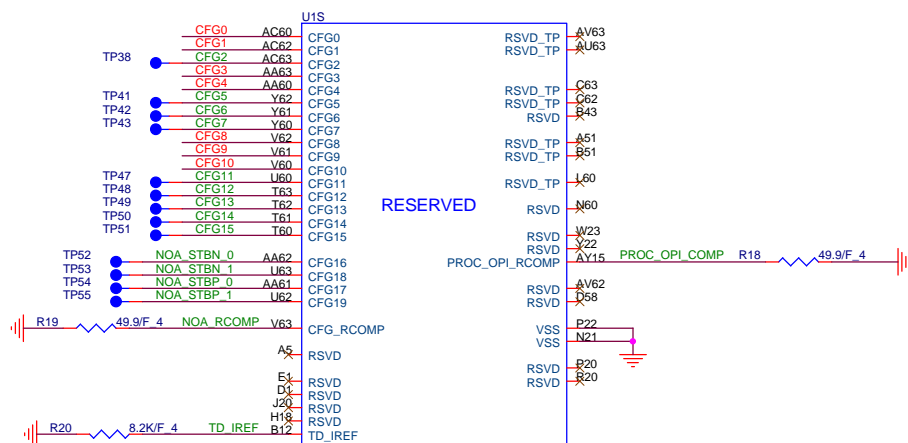
PROJECT : HKDD

Size	Document Number	Rev
	HSW MCP(Display/eDP)	1A

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Date: Monday, November 10, 2014 Sheet 4 of 41

[illegible]



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	



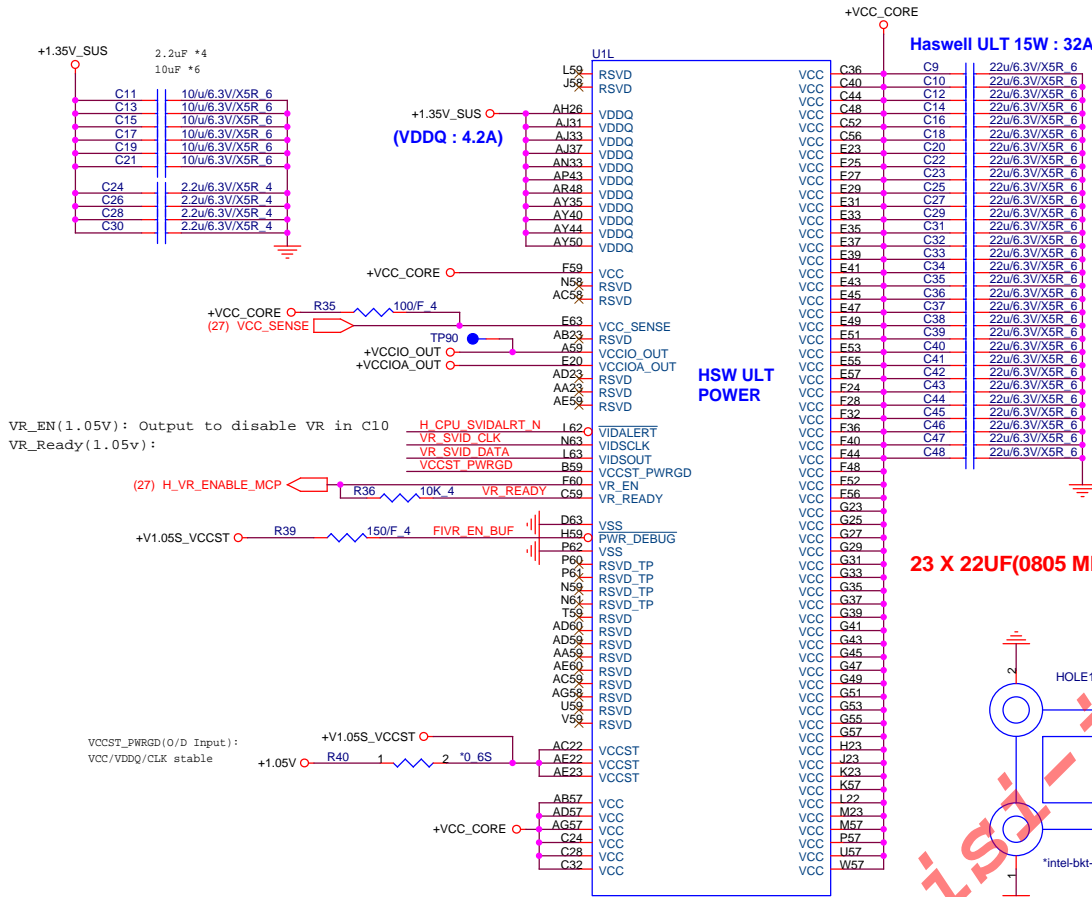
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PROJECT : HKDD

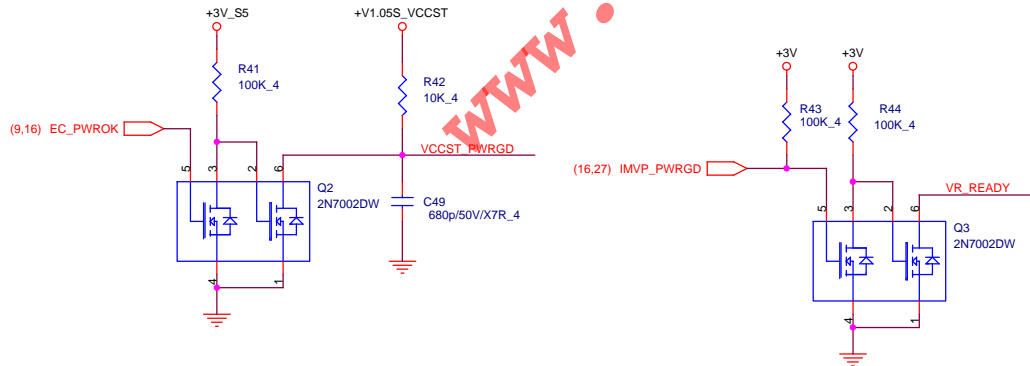
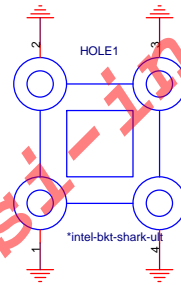
Size	Document Number	Rev
	HSW MCP(CFG)	1A
Date:	Monday, November 10, 2014	Sheet 6 of 41

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

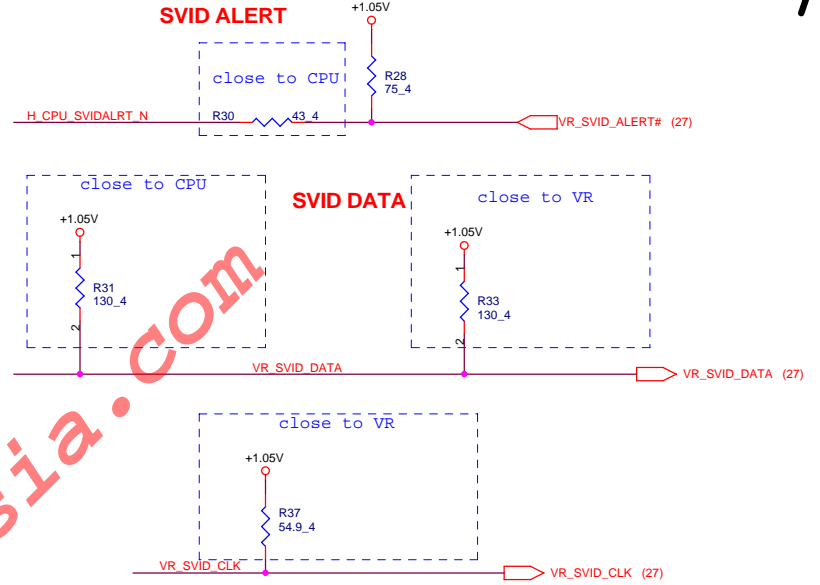
Haswell ULT MCP (POWER)



23 X 22UF(0805 MLCC)



SVID ALERT



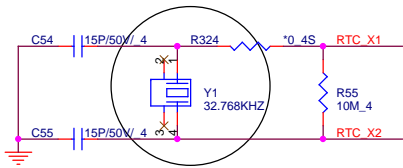
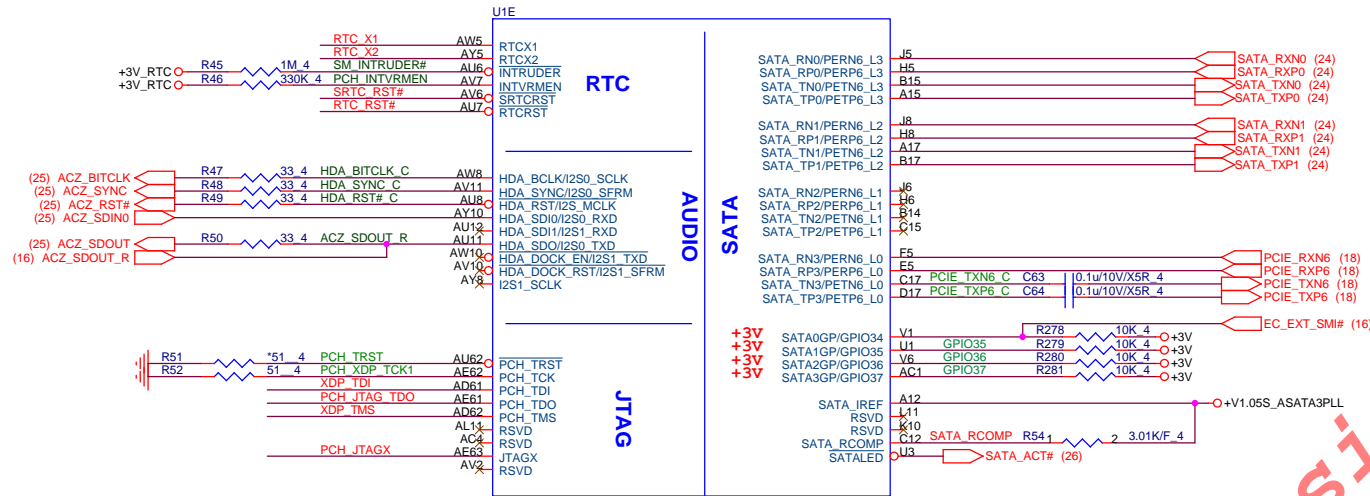
Quanta Computer Inc.

PROJECT : HKDD

Size	Document Number	Rev
	HSW MCP(Power)	1A

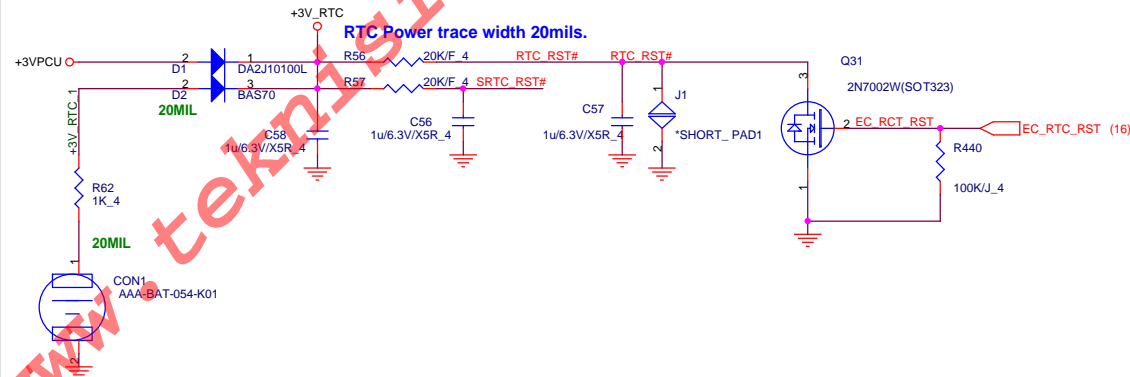
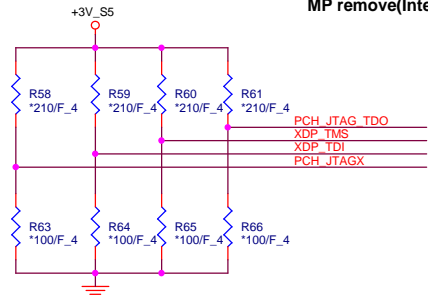
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Date: Monday, November 10, 2014 Sheet 7 of 41



PCH JTAG Debug (CLG)

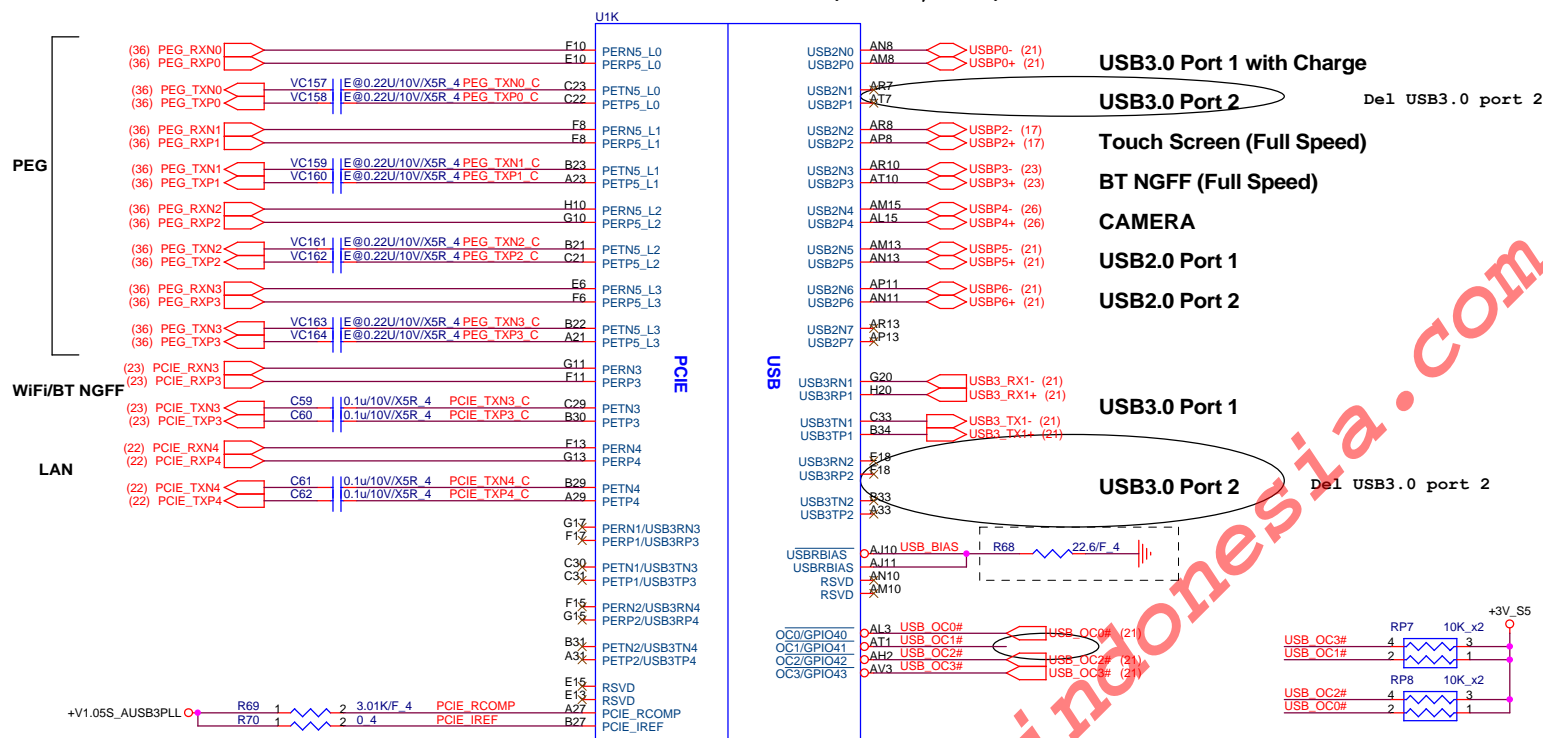
MP remove(Intel)



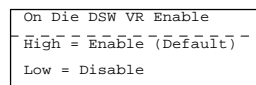
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V ○ R67 1K 4 SPKR (11,25)
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTVRMEN	Mode Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	

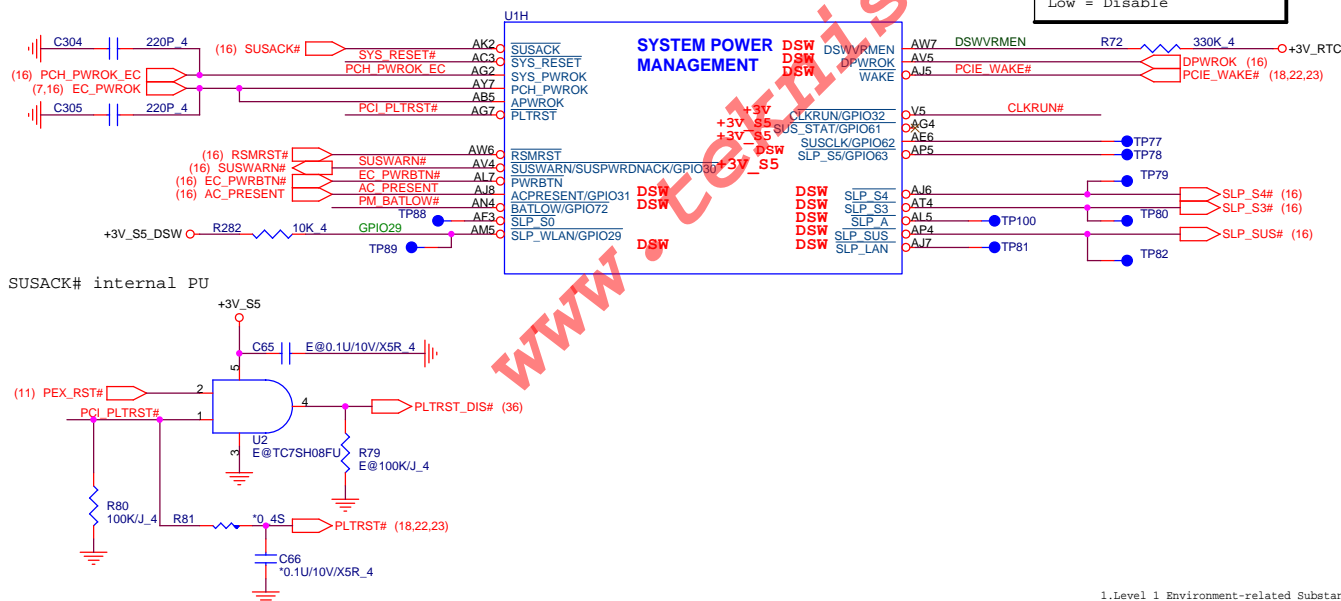
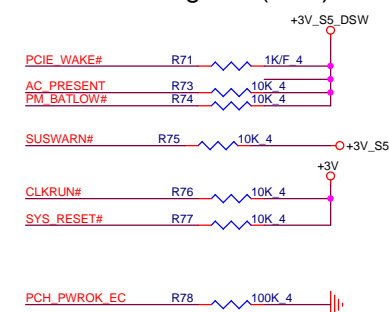
Haswell ULT (PCIe, USB)



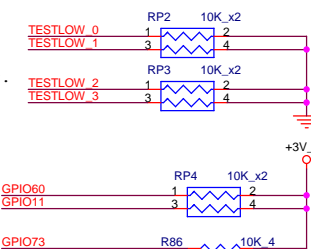
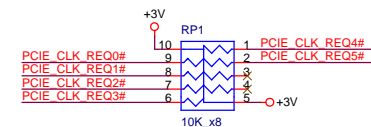
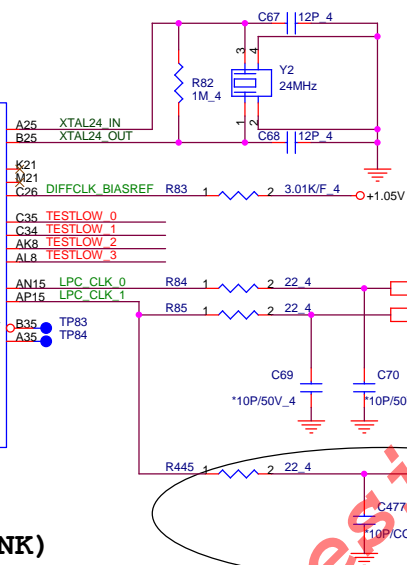
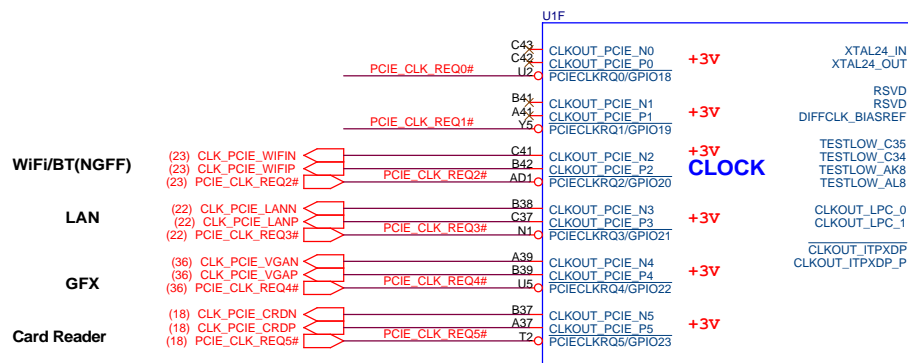
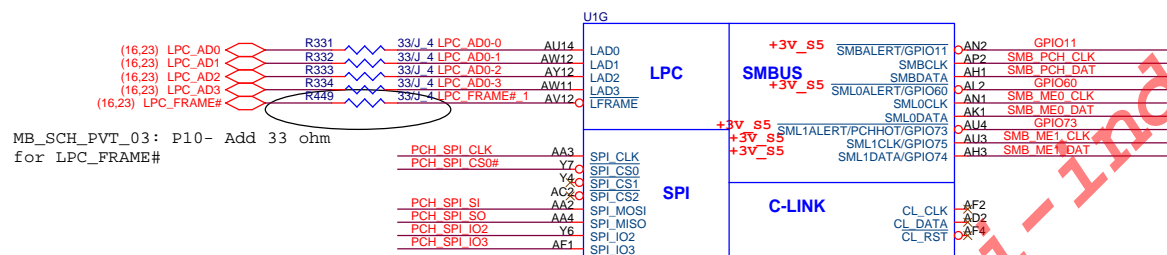
Haswell ULT (SYSTEM POWER MANAGEMENT)



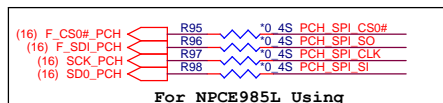
PCH Pull-high/low(CLG)



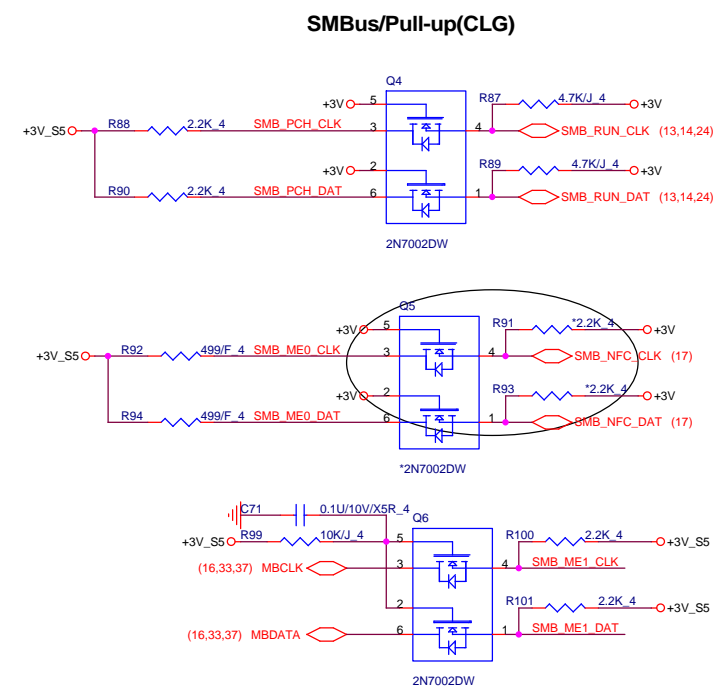
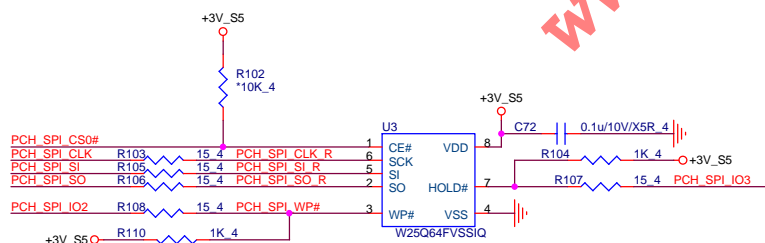
Haswell ULT (CLK)

**Haswell ULT (LPC/SPI/SMB/CLINK)**

MB_SCH_PVT_03: P10- Add 33 ohm
for LPC FRAME#



SPI FLASH



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PROJECT : HKDD

ber	Rev
HSW PCH(CI K/I PC/SPI/SMB)	1A

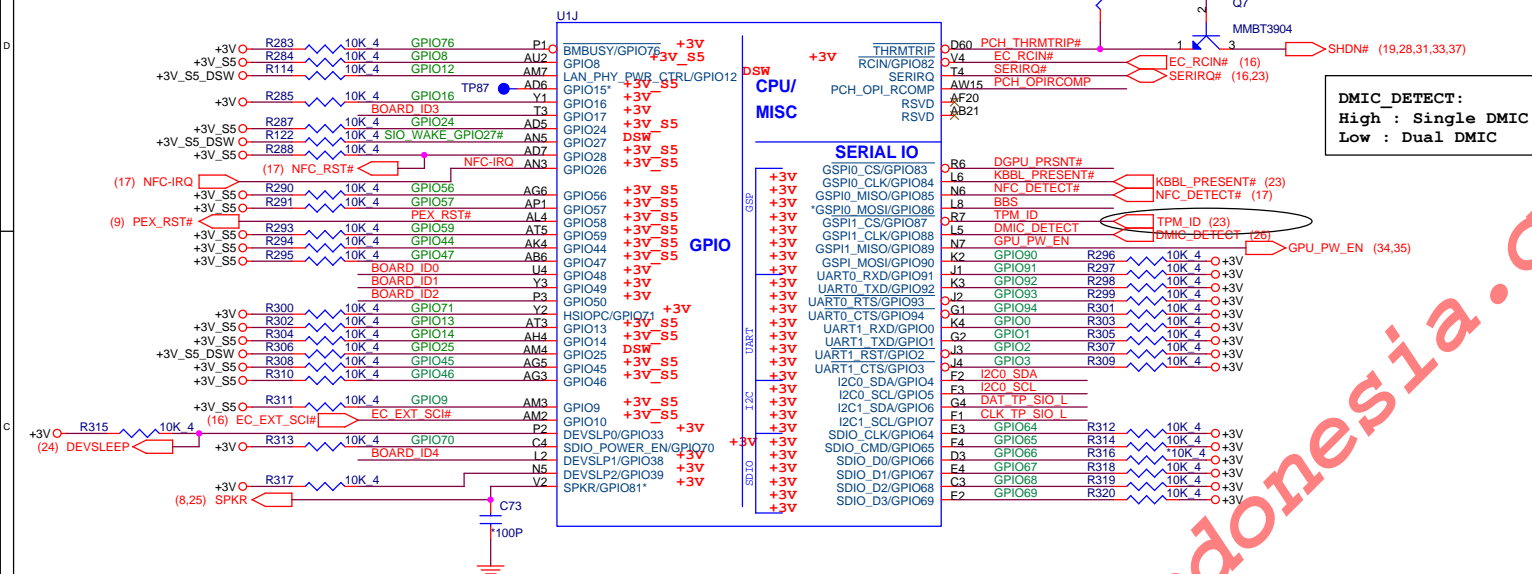
- 1.Level 1 Environment-related Substances Should Never be Used.
- 2.Recycled Resin and Coated Wire should be procured from Green Partners.

Size	Document Number	Rev
	HSW PCH(CLK/LPC/SPI/SMB)	1A
Date:	Wednesday, November 12, 2014	Sheet 10 of 41

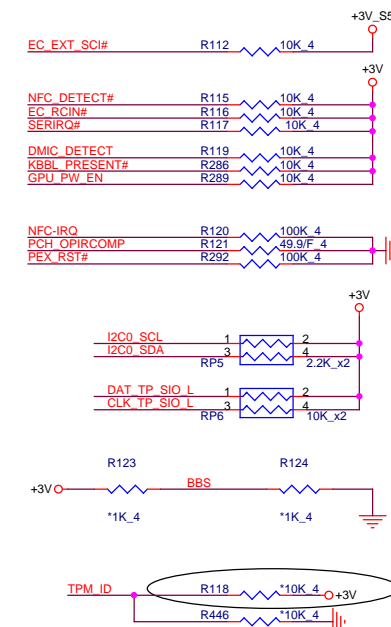
Hasswell ULT (GPIO, LPIO, MISC)

GPI027

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx



GPIO Pull-up/Pull-down(CLG)



GPIO66 Top-Block Swap	
PU	Enable
PD	Disable(Default) internal weak pull-dpwn

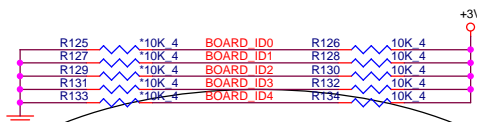
GPIO86	
PU	LPC
PD	SPI (Default IPD)

No Reboot Strap(GPIO81)	
NC	Default
PU	EN

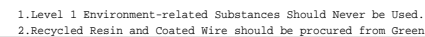
TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN

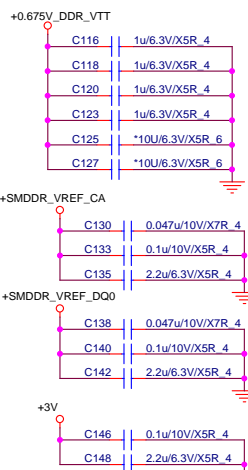
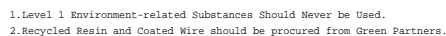
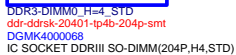
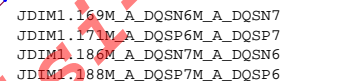
 Quanta Computer Inc PROJECT : HKDD	
Size	Document Number HSW PCH(GPIO/MISC)

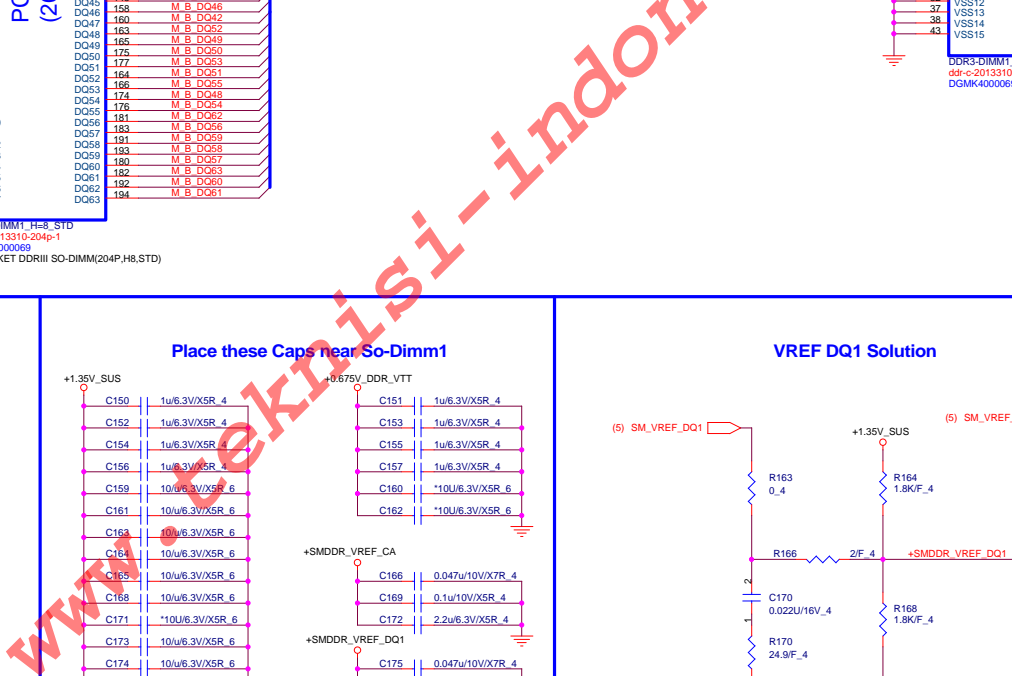
MB_SCH_PVT_04: P11- Add BOARD ID table



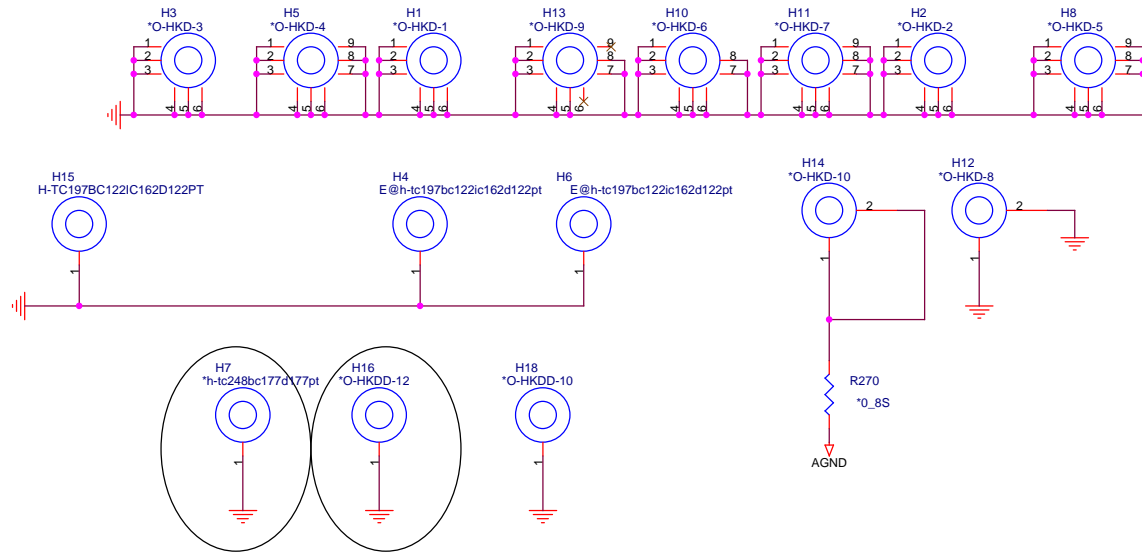
PCBA SKU	Discrete	UMA
R135(Pull High)	Stuff	No Stuff
R136(Pull Low)	No Stuff	Stuff



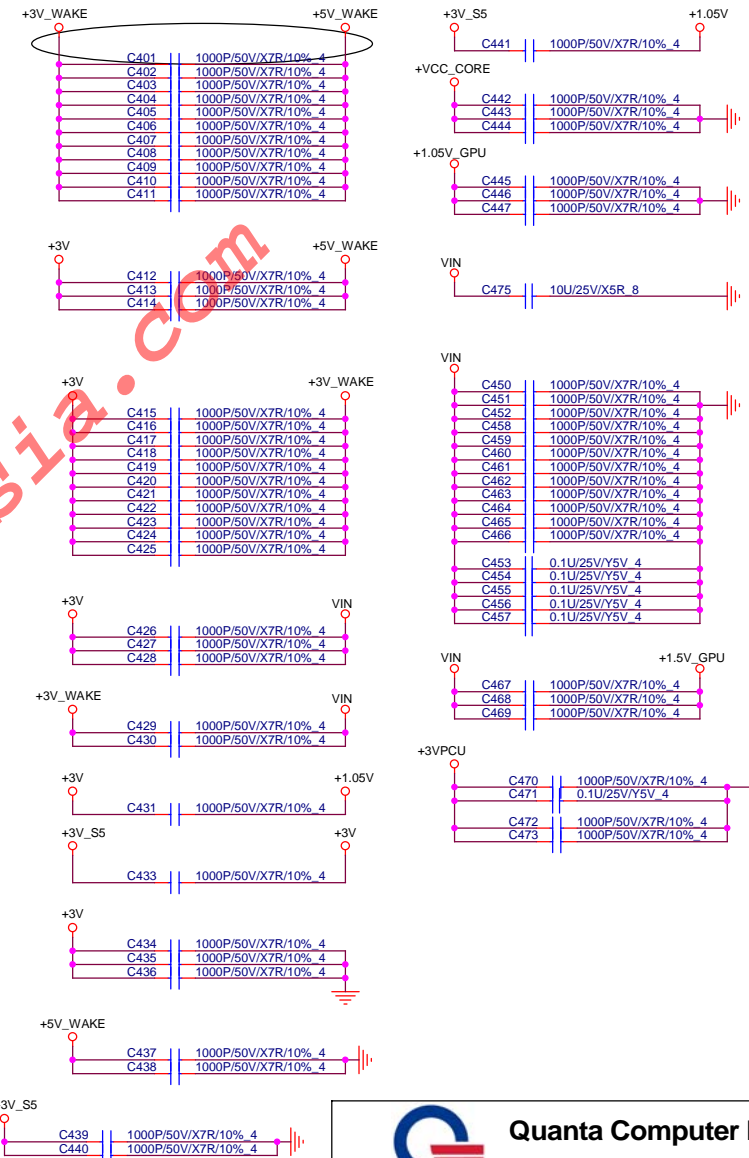
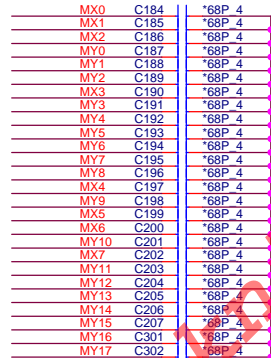
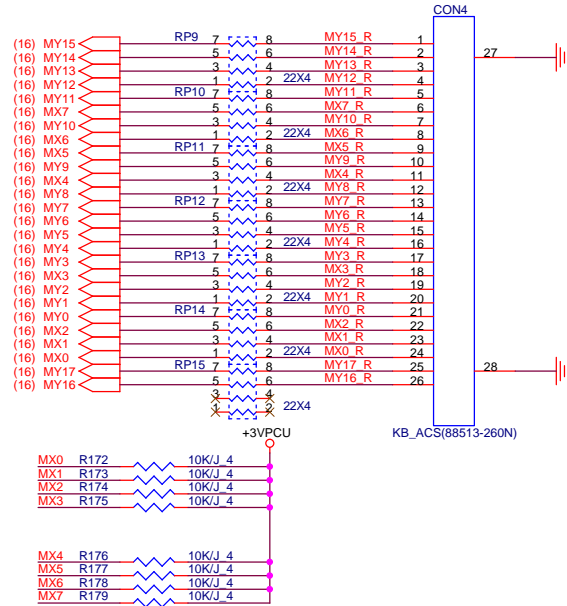




VREF DQ1 Solution

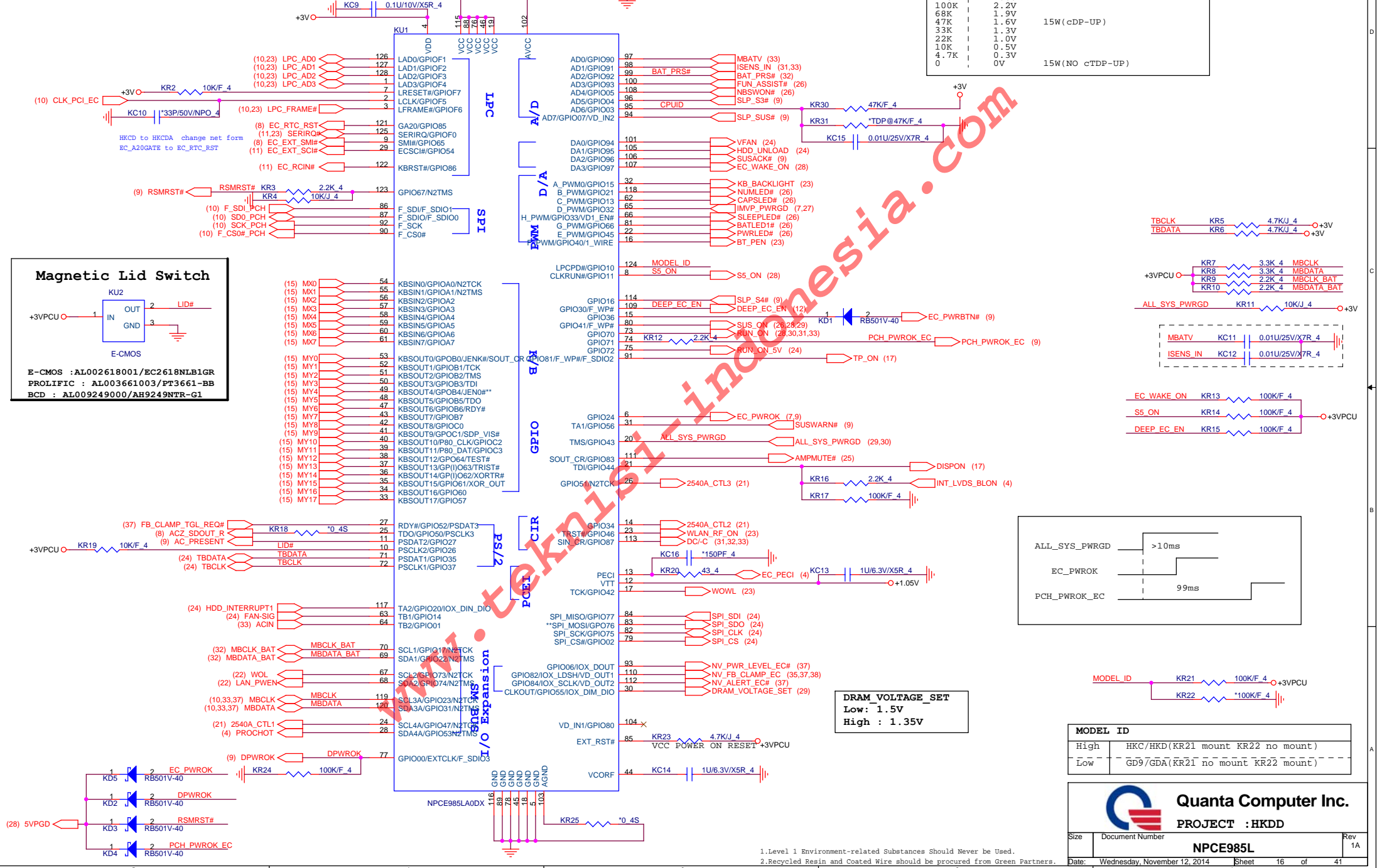


KEY BOARD Connector

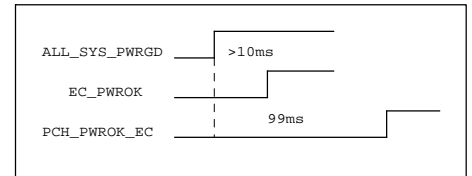
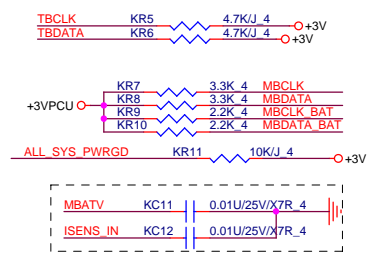
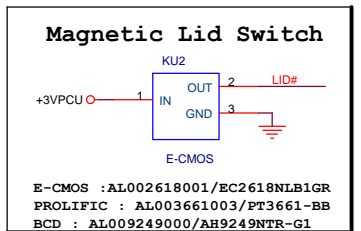


New ADD
**** Strapping Pin, Can not pull low.**
Note the input leakage current to the strap pins must be less than 10uA.

Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default



KR31	CPUID	TDP
X	3.3V	28W
470K	2.9V	TDB
220K	2.6V	
100K	2.2V	
68K	1.9V	15W (cDP-UP)
47K	1.6V	
33K	1.3V	
22K	1.0V	
10K	0.5V	
4.7K	0.3V	15W (NO cTDP-UP)
0	0V	



DRAM VOLTAGE SET
 Low : 1.5V
 High : 1.35V

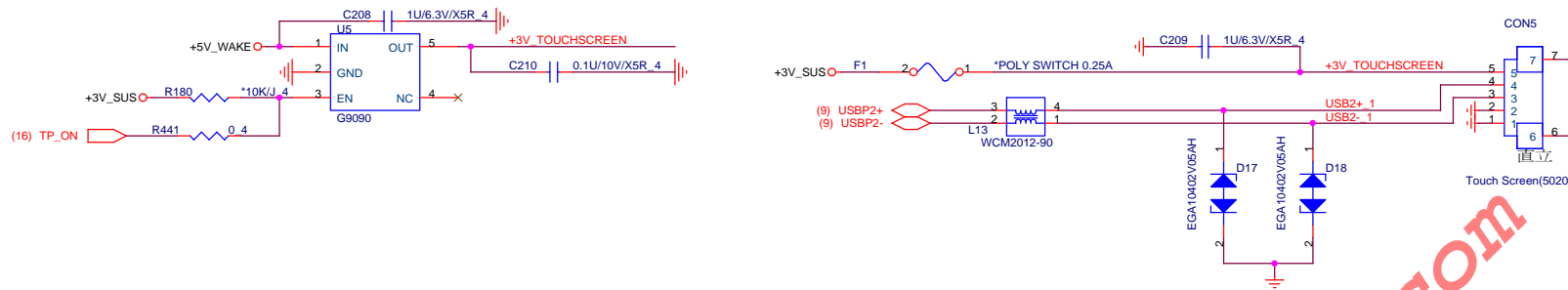
MODEL ID	
High	HKC/HKD(KR21 mount KR22 no mount)
Low	GD9/GDA(KR21 no mount KR22 mount)

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PROJECT : HKDD

Size	Document Number	NPCE985L	Rev	1A
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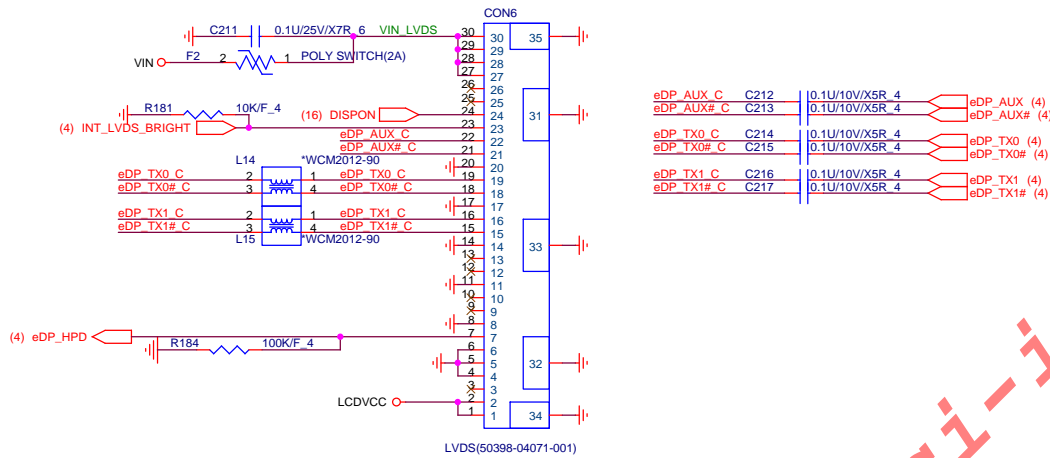
1.Level 1 Environment-related Substances Should Never be Used.
 2.Recycled Resin and Coated Wire should be procured from Green Partners.

Touch Screen

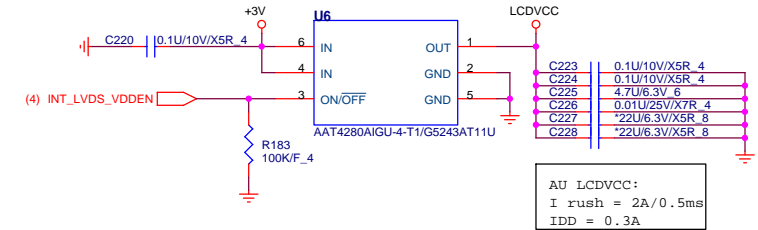


FAST, UL/CSA

eDP

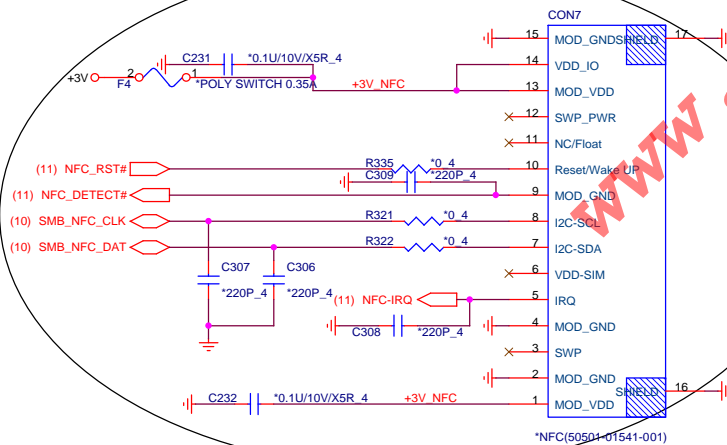


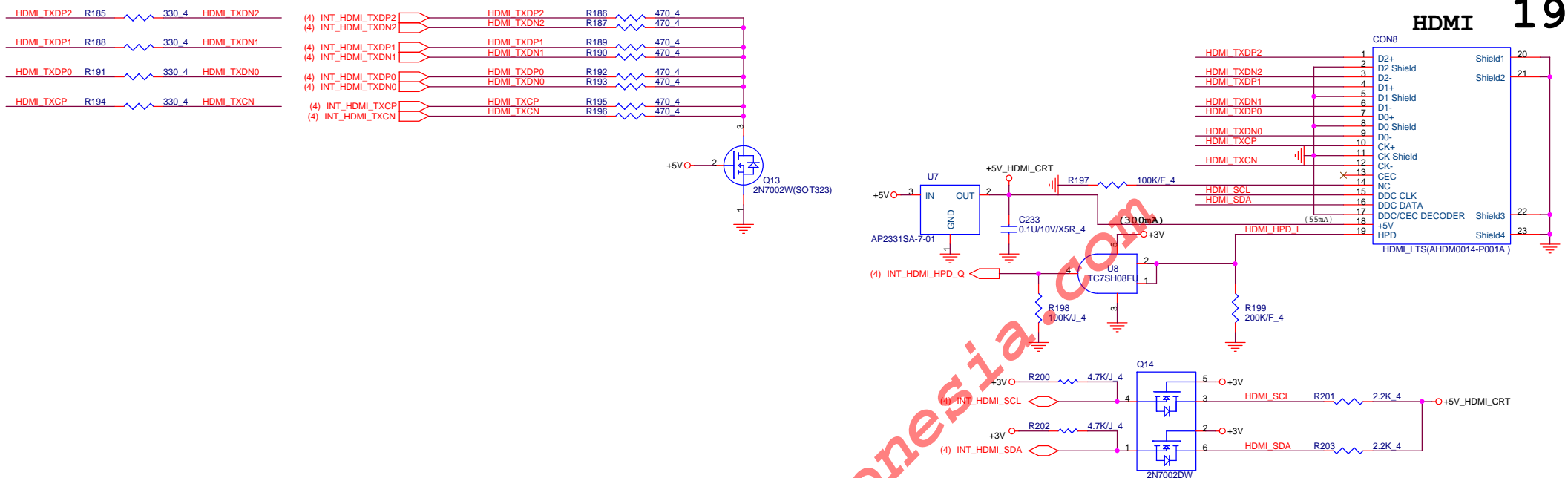
NB LVDS enable



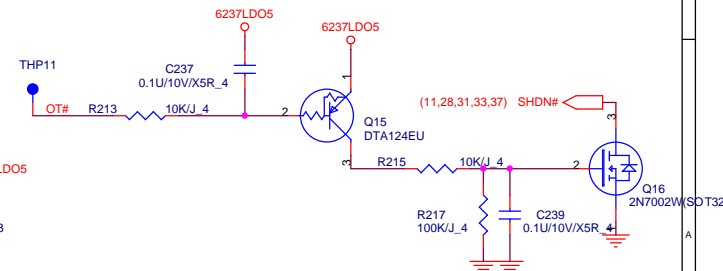
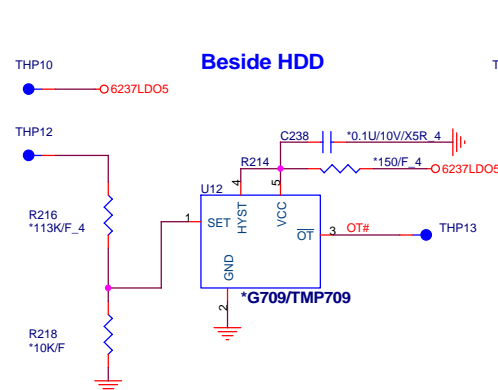
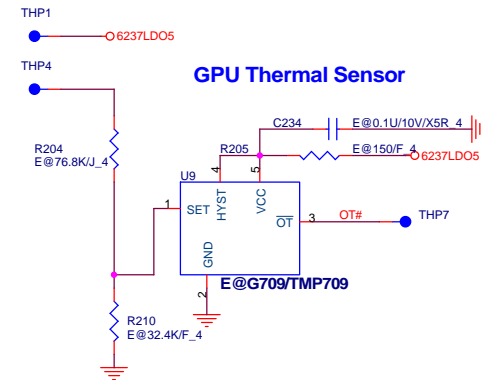
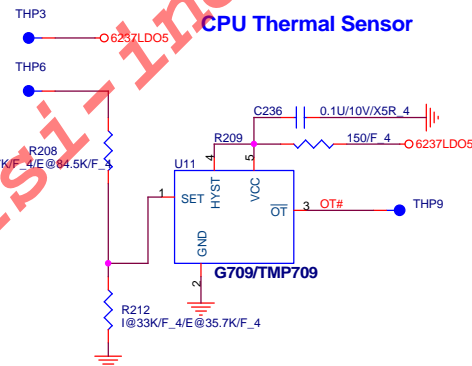
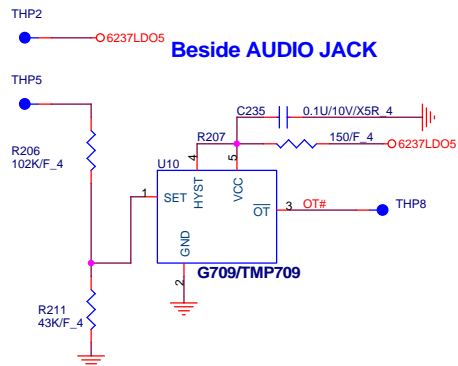
AU LCDVCC:
I_{rush} = 2A/0.5ms
IDD = 0.3A

NFC





H/W Thermal Protect



$$RSET(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$$

95	18.5K
100	15K
107	10.3K
110	8.2K

DIS SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	72	R212=35.35K	35.7K	72.1	71.1
Near GFX sensor temp	76	R210=40.72K	32.4K	76.4	75.4
Near AUDIO sensor temp	62	R211=43.05K	43K	62	61

UMA SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	81	R212=33.09K	33K	82.3	81.4
Near AUDIO sensor temp	58	R211=43.05K	43K	62	61

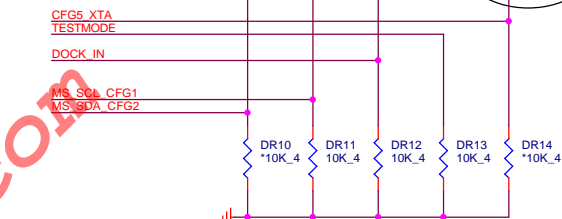
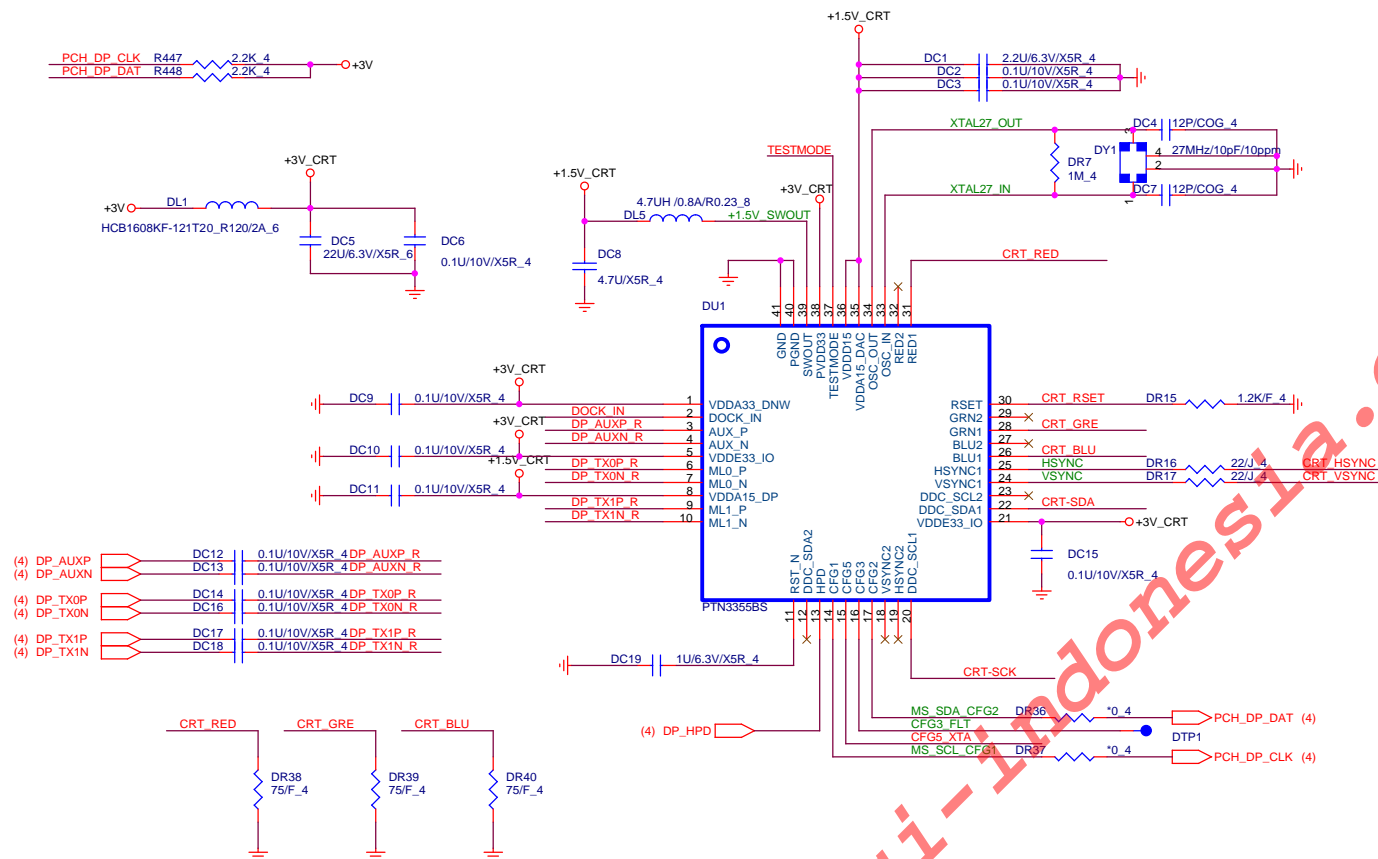


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PROJECT : HKDD

Size	Document Number	Date	Thursday, November 13, 2014	Sheet	19	of	41
HDMI/Thermal IC							

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

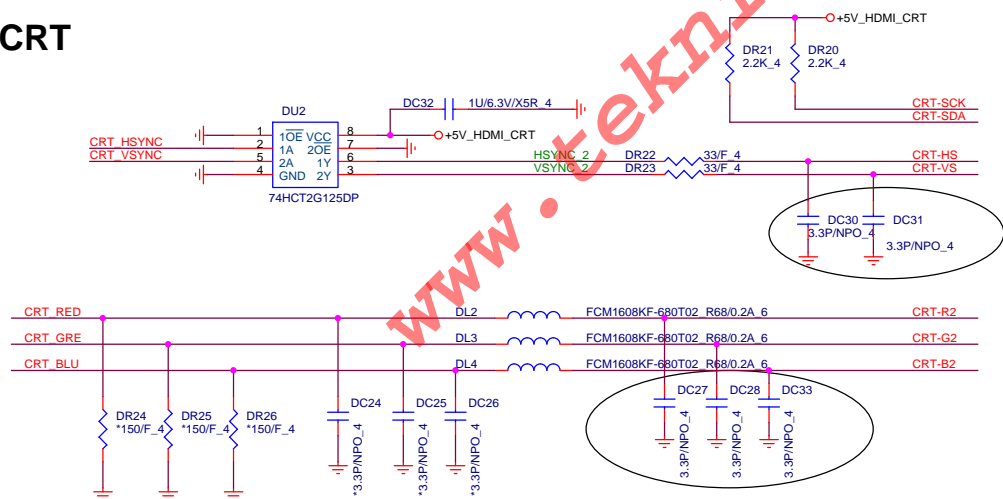


CFG5_XTA	XTAL is used, High=33MHZ, Low=25MHZ, NC=27MHZ
TESTMODE	I2C address, Stuff=C0H, NC=40H
DOCK_IN	High=Channel 2, Low=Channel 1
MS_SCL_CFG1	General purpose configuration pin
MS_SDA_CFG2	General purpose configuration pin
CFG3_FLT	Open: not used

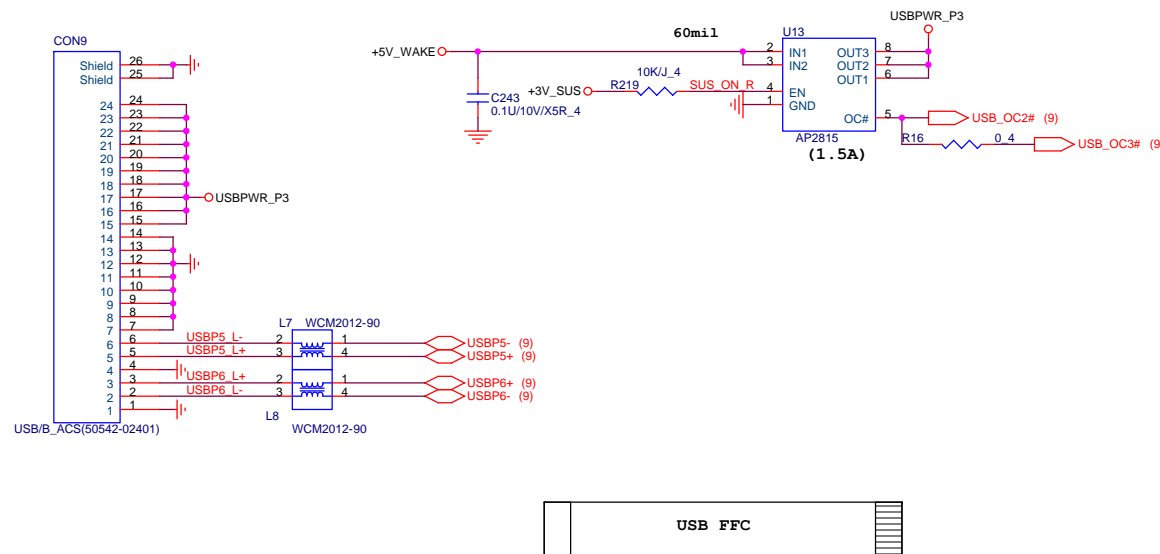
Table 6. CFG1_SCL/CFG2_SDA pin definitions

Pin value	System behavior
00	Compliant HPD behavior
01	Most interoperable (non-compliant) HPD behavior
10	Most interoperable (non-compliant) HPD behavior
11	(Default) Compliant behavior (but configurable via PC-bus)

CRT



MB to USB board

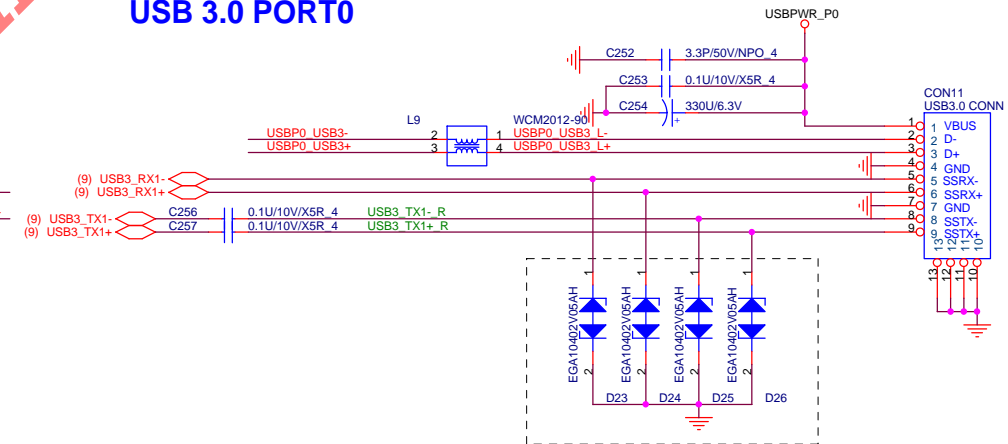
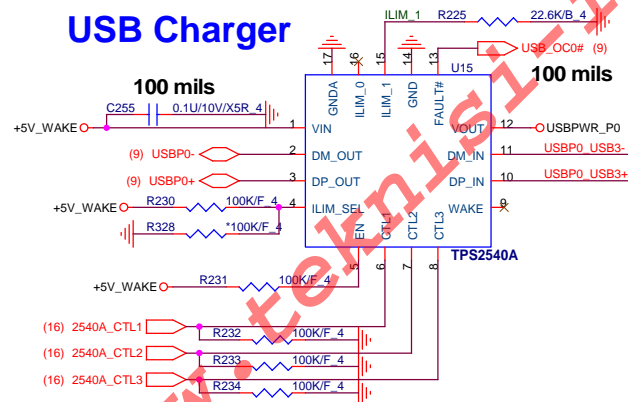
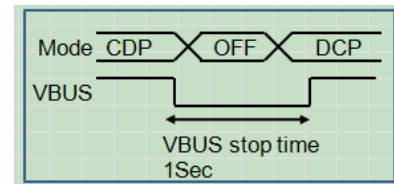


USB 3.0 PORT0

USB Charger

	TPS2540A		TPS2543	
ILIM_SEL	Pin15	Pin16	Pin15	Pin16
High	V			V
Low		V	V	


SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS



CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP, Auto-detect(S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	1	1	CDP (S0, 1.5A)

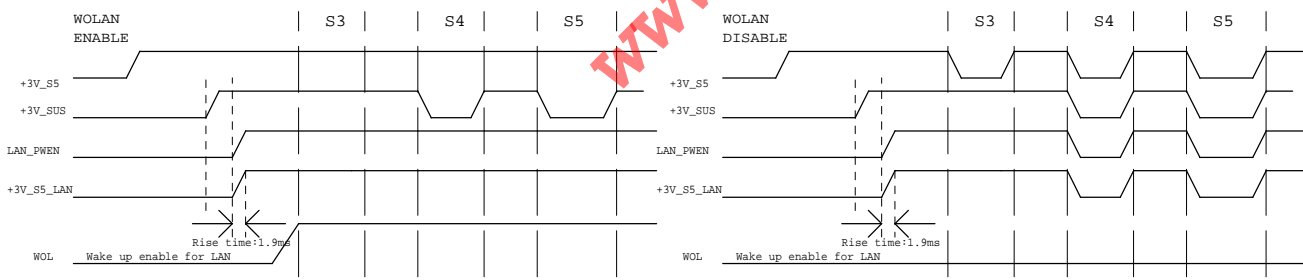
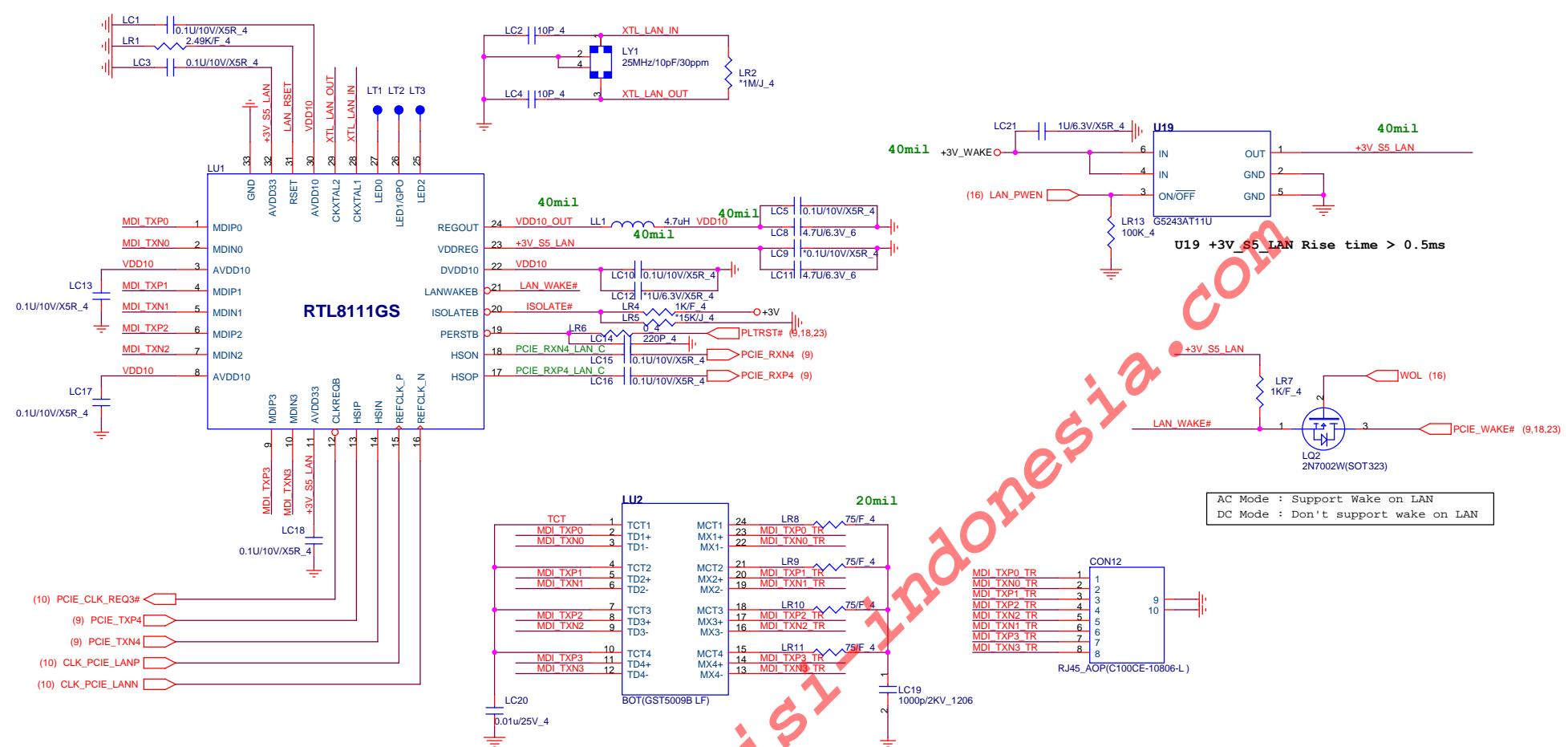
System State	USB Battery Charging Setting			
	Disable	C(1 2 3)	Enable	C(1 2 3)
S0				
S3	SDP	(X 1 0)	CDP	(1 1 1)
DS3	SDP	(X 1 0)	DCP BC	(1 0 0)
S4	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S5	Charger OFF	(0 0 0)	DCP BC	(1 0 0)

ILIM_SEL		(I LIMIT(A)= 48000/R)
HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A


**Quanta Computer Inc.**
PROJECT : HKDD
USB/USB Charger

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1. Level 1 Environment-Related Substances should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.



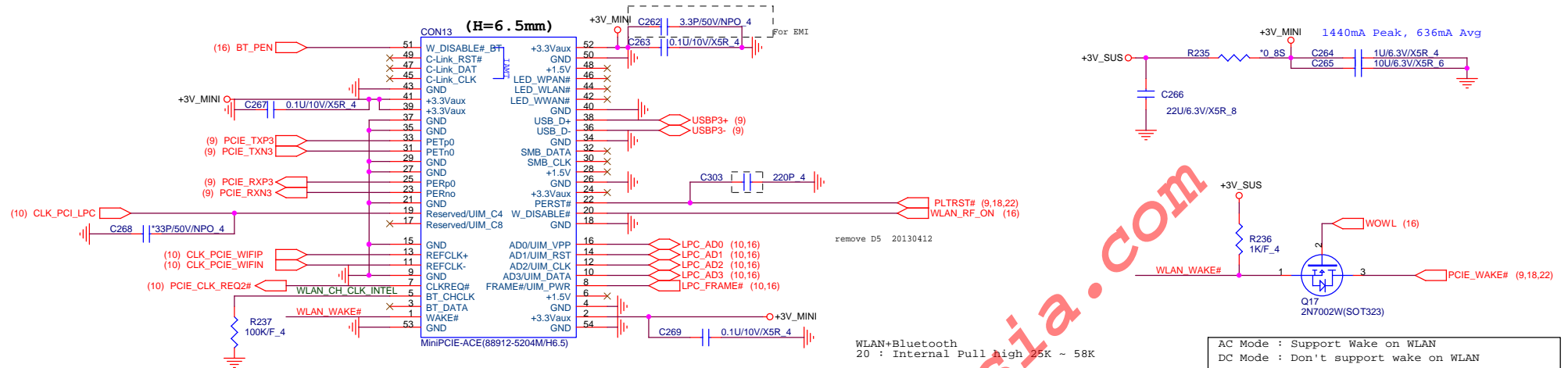
BIOS Setup	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	H	H	H
S4	L	L	H	H
S5	L	L	H	H

**Quanta Computer Inc.**
PROJECT : HKDD
Giga LAN RTL8111GS

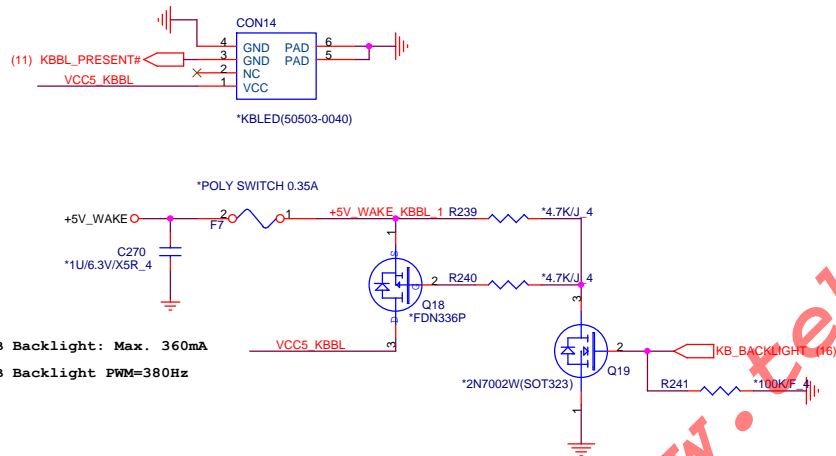
Size	Document Number	Date	Thursday, November 13, 2014	Sheet	22	of	41	Rev	1A
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1.Level 1 Environment-related Substances Should Never be Used.
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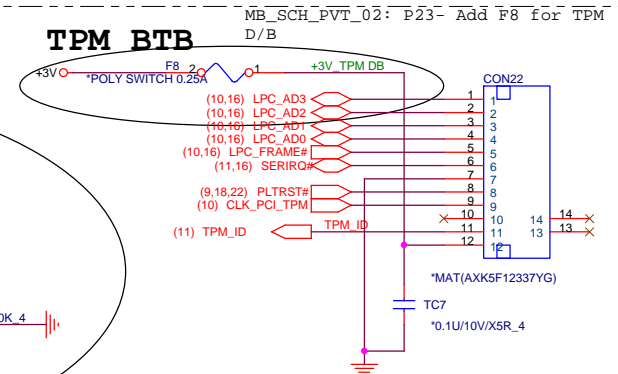
WLAN/WIMAX/WIDI



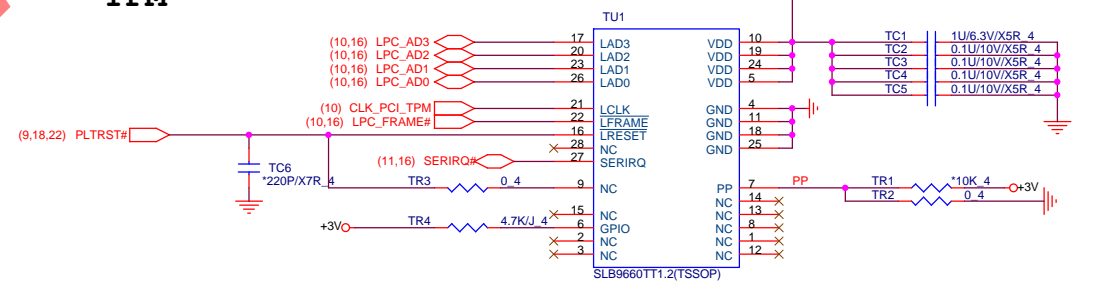
KB BACKLIGHT



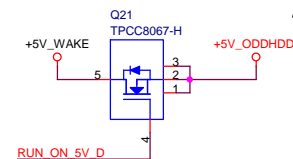
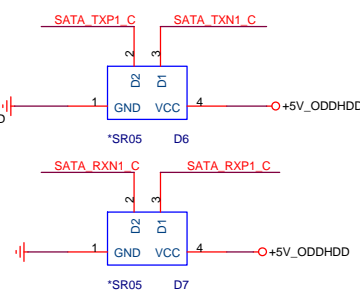
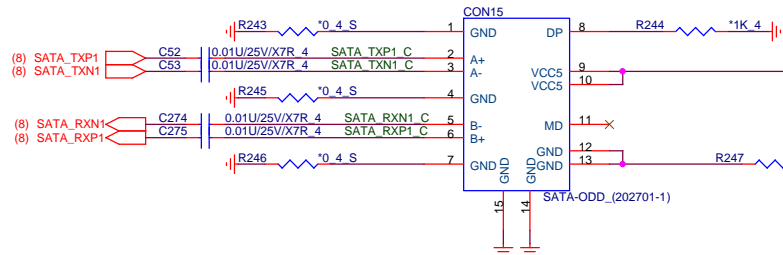
TPM BTB



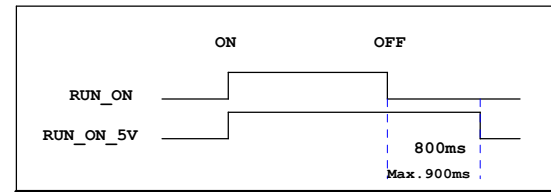
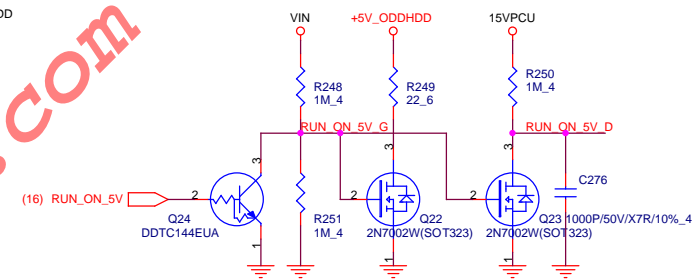
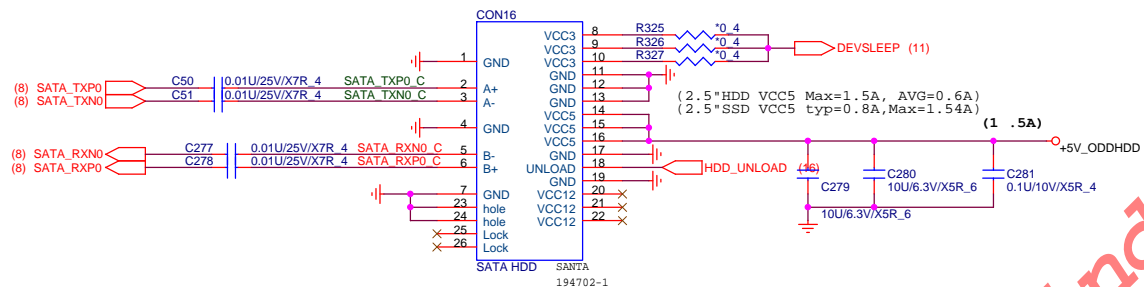
TPM



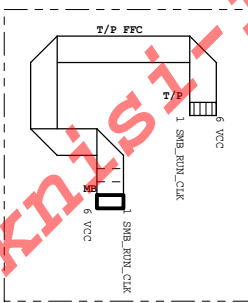
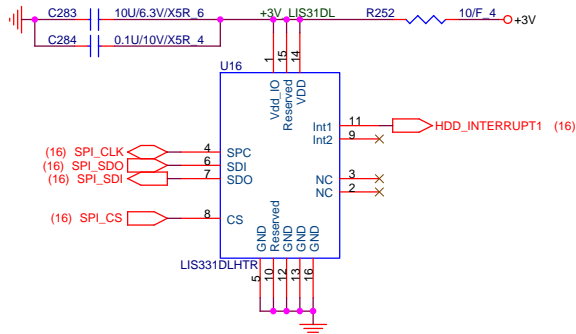
ODD CONNECTOR



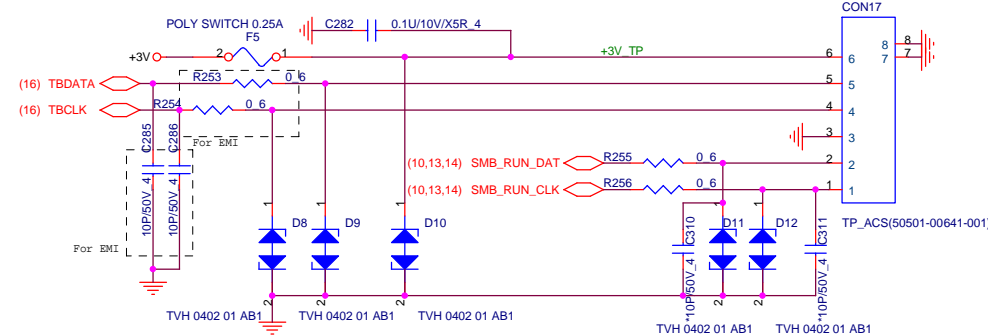
HDD CONNECTOR



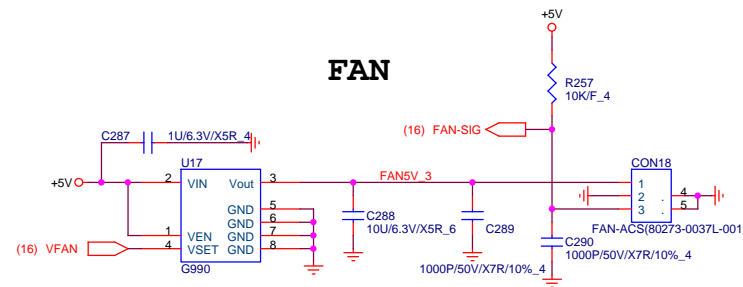
HDD PROTECT SPI INTERFACE



T/P Board to T/P



FAN



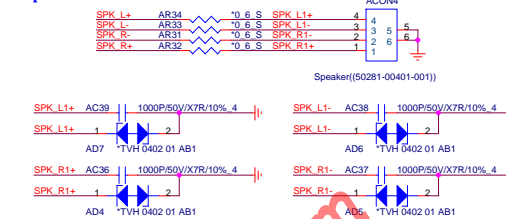
Analog

Digital

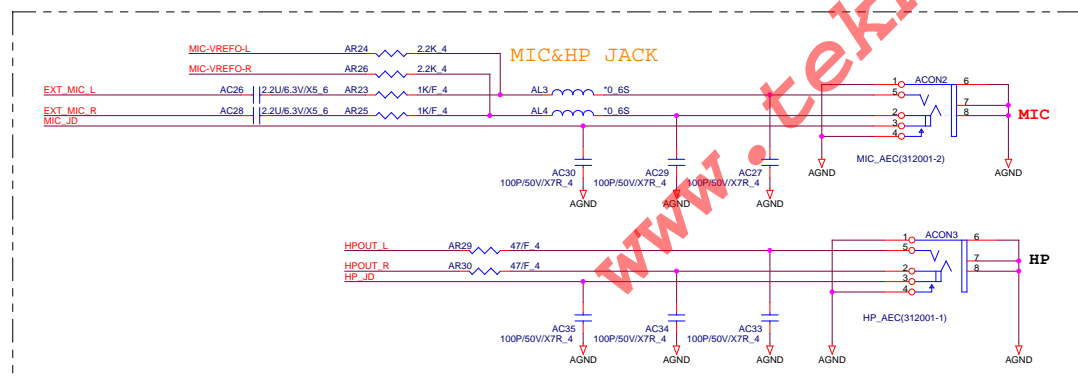
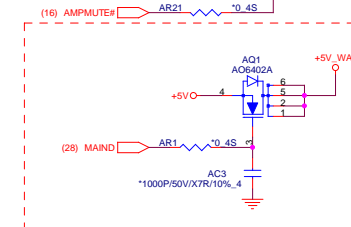
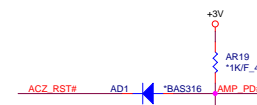
ALC233-CG

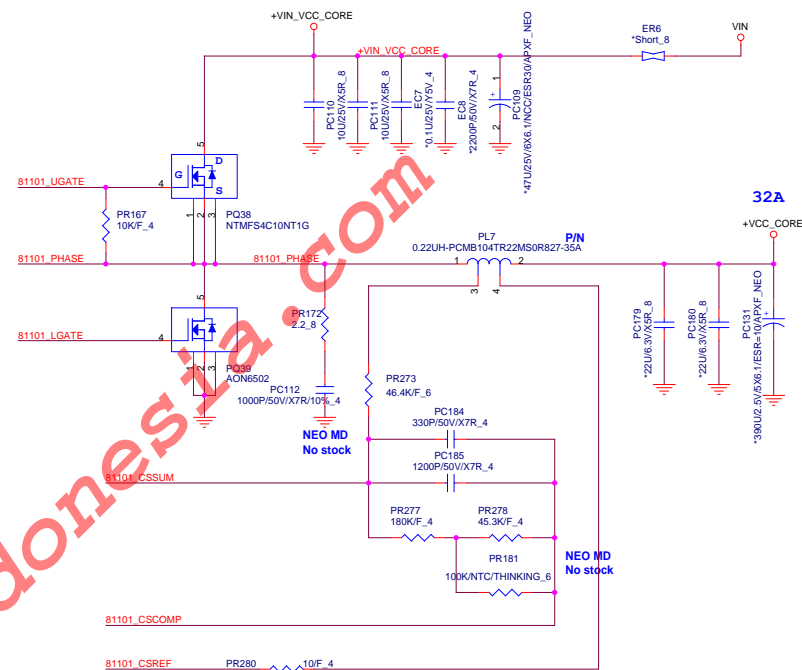
SPK L+ L- R+ R- trace width
Speaker 4 ohm => 40 mils

SPEAKER CON.

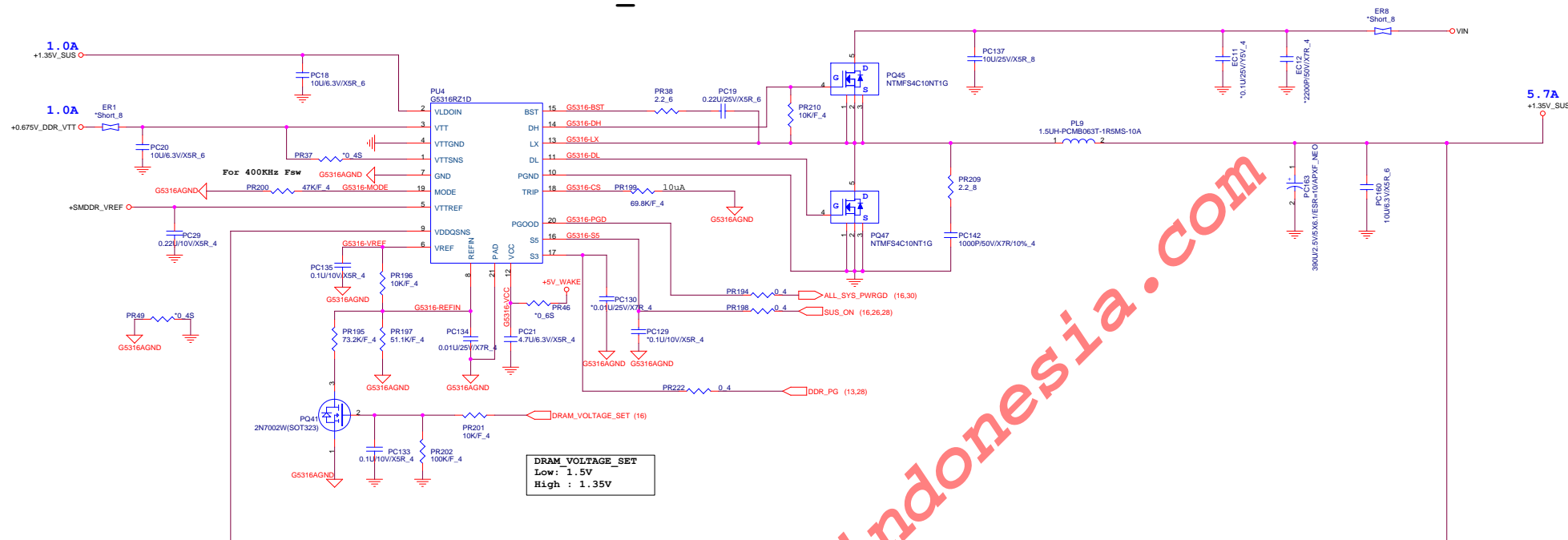
<<Attention>>
Place these EMI components close to codec; For EMI issue.

For EMI





1.5VSUS & VTT_MEM

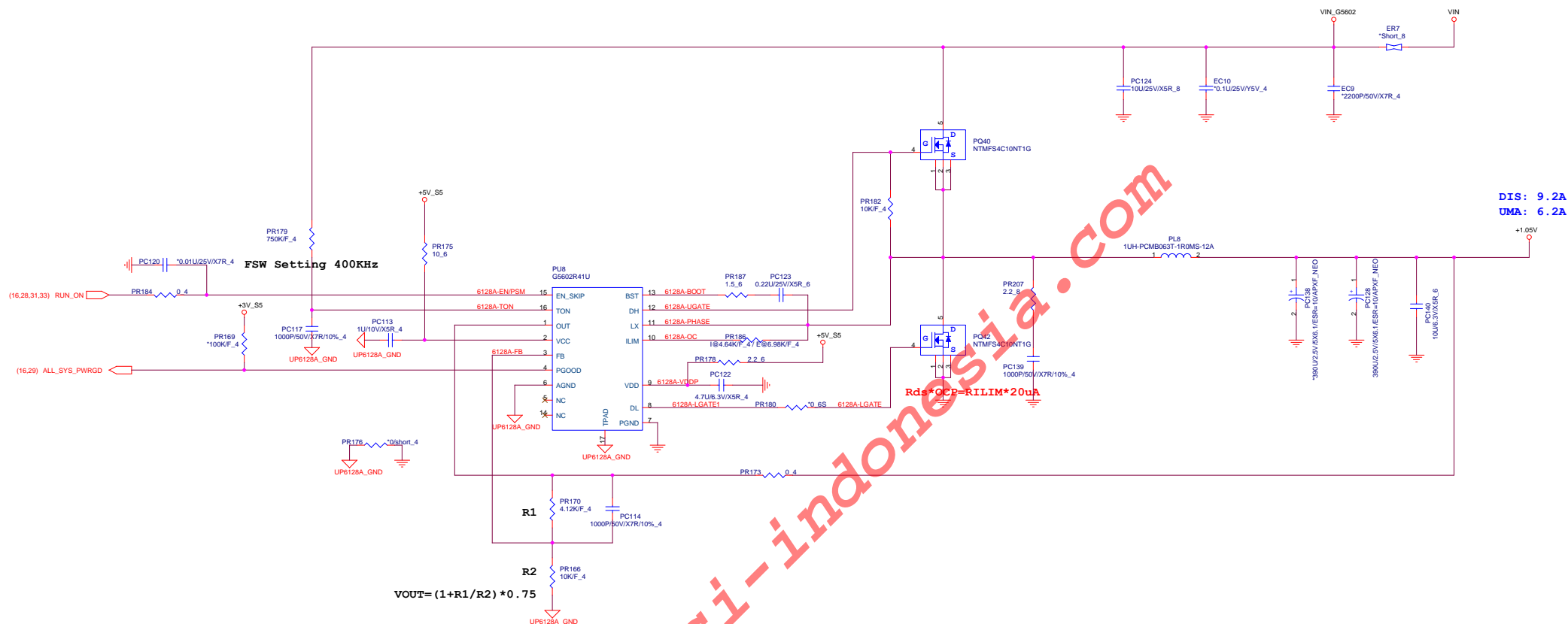


MODE	Resistor on Mode	Faw	Discharge Mode
3	200Kohm	400KHz	Tracking discharge
2	100Kohm	300KHz	
1	68Kohm	300KHz	Non-tracking discharge
0	47Kohm	400KHz	

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off



+1.05V



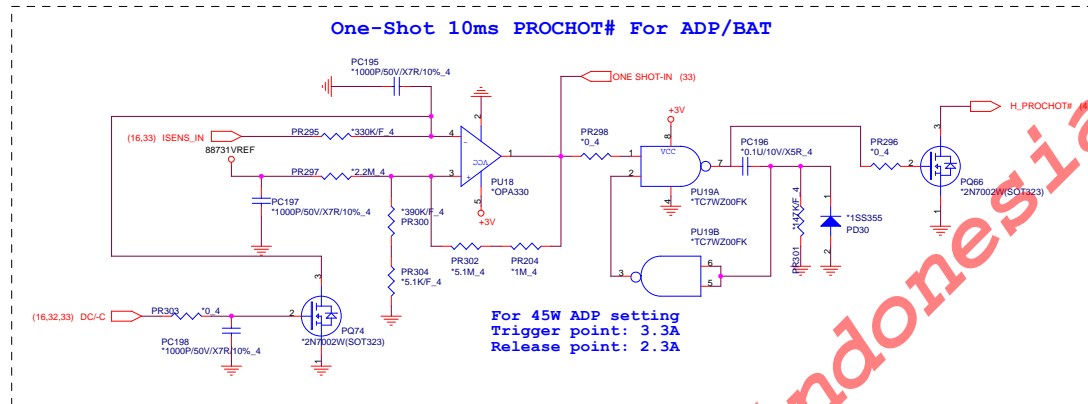
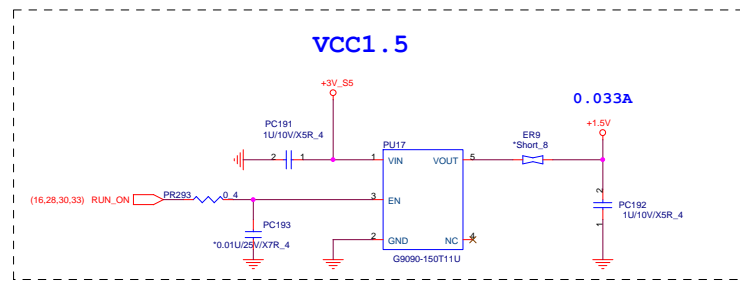
Quanta Computer Inc.
PROJECT : HKDD

Size	Document Number	Rev
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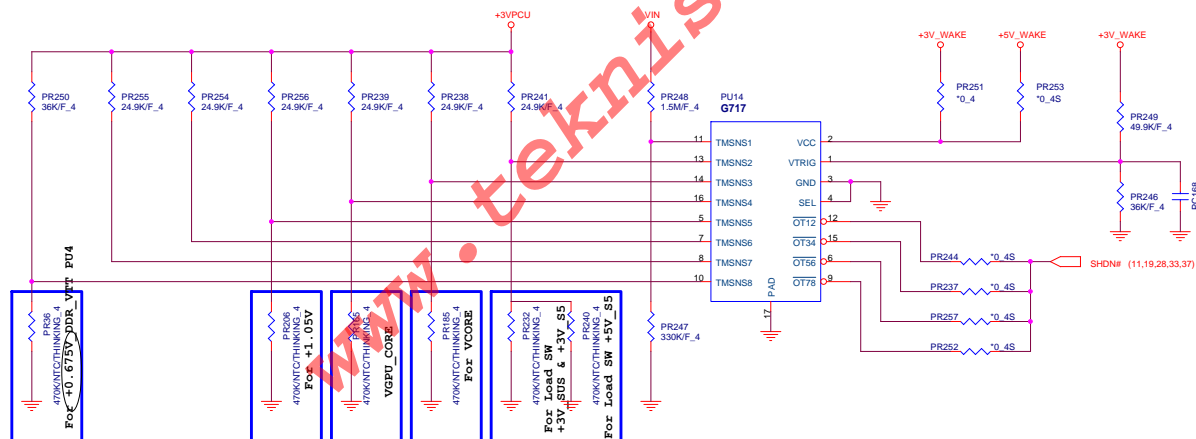
1. Level 1 Environment-related Substances Should Never be Used.

2. Recycled Resin and Coated Wire should be procured from Green Partners.

Date: Monday, November 10, 2014 Sheet 30 of 41



Thermal Protection and Battery UVP for VEDS

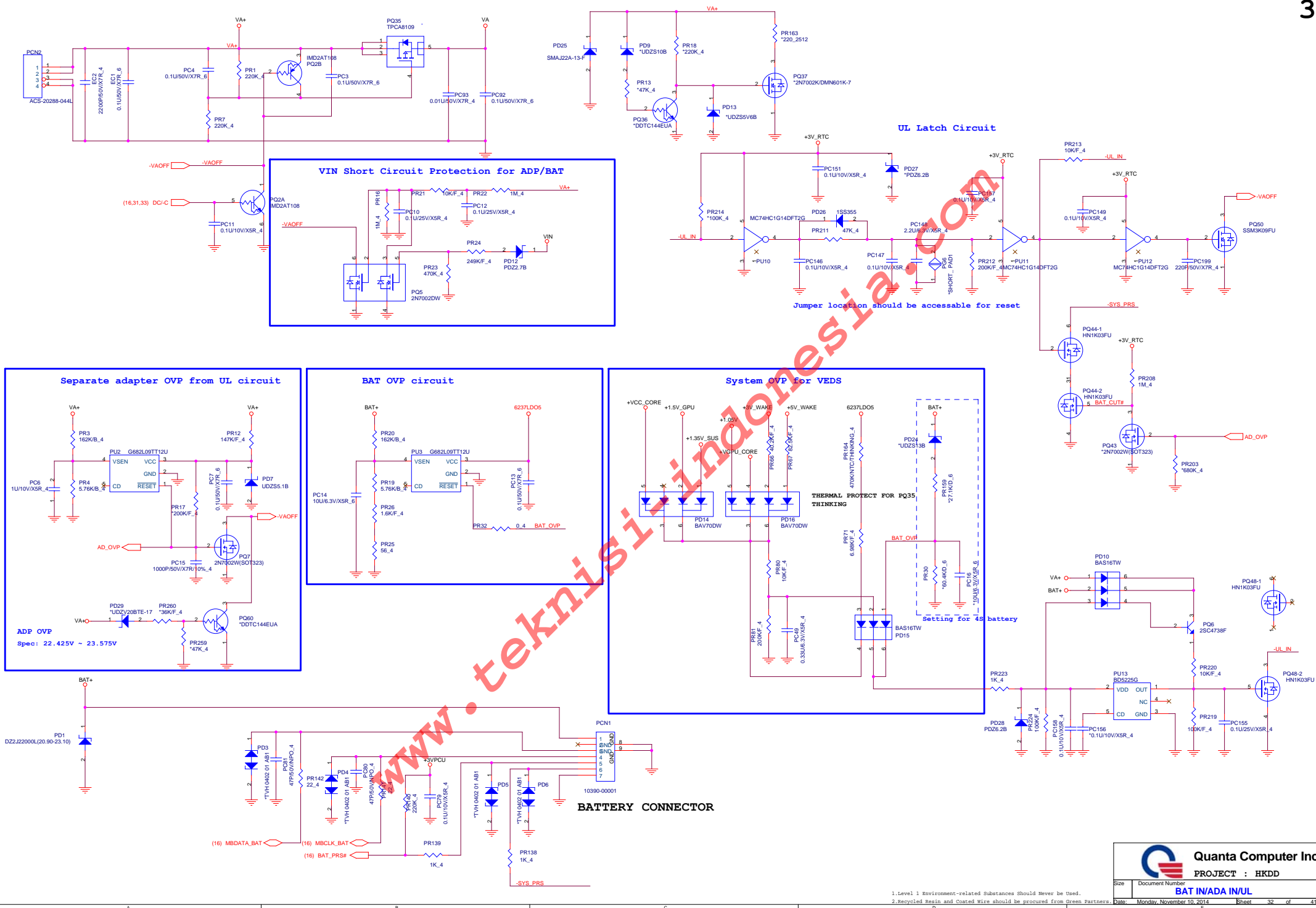


Quanta Computer Inc.
PROJECT : HKDD

Size	Document Number	Rev
	VCC1.8	1A

1. Level 1 Environment-related Substances Should Never be Used.
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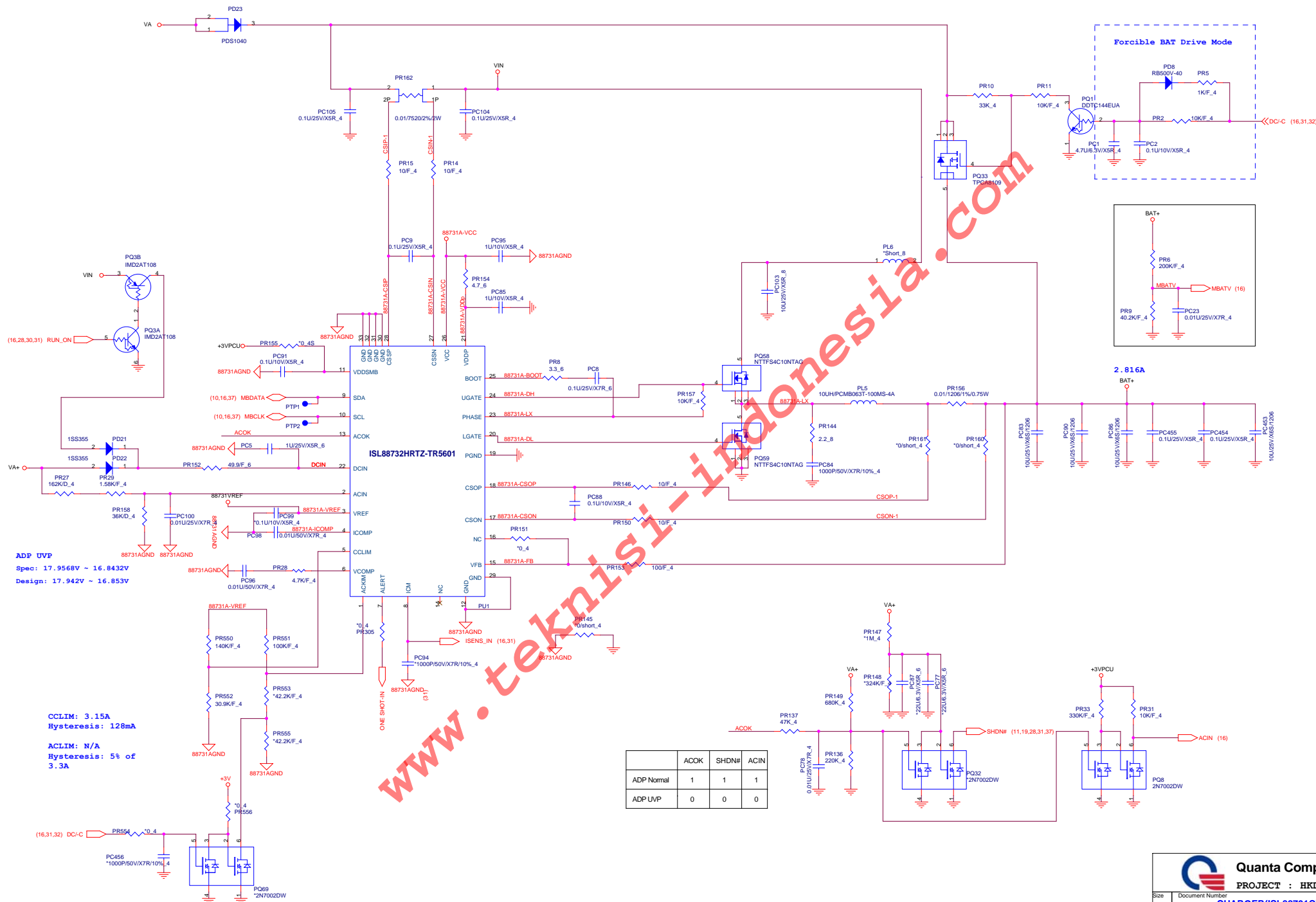
Quanta Computer Inc.
PROJECT : HKDD

Size Document Number
BAT IN/ADA IN/UL
Rev 1A

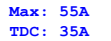
1. Level 1 Environment-related Substances Should Never be Used.

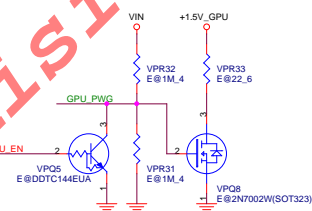
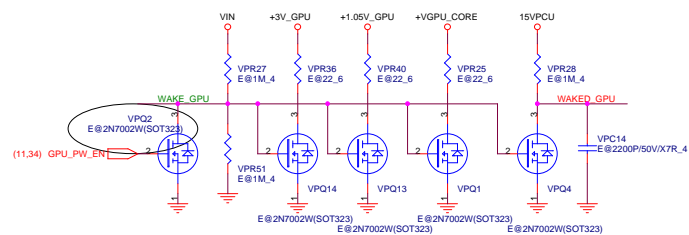
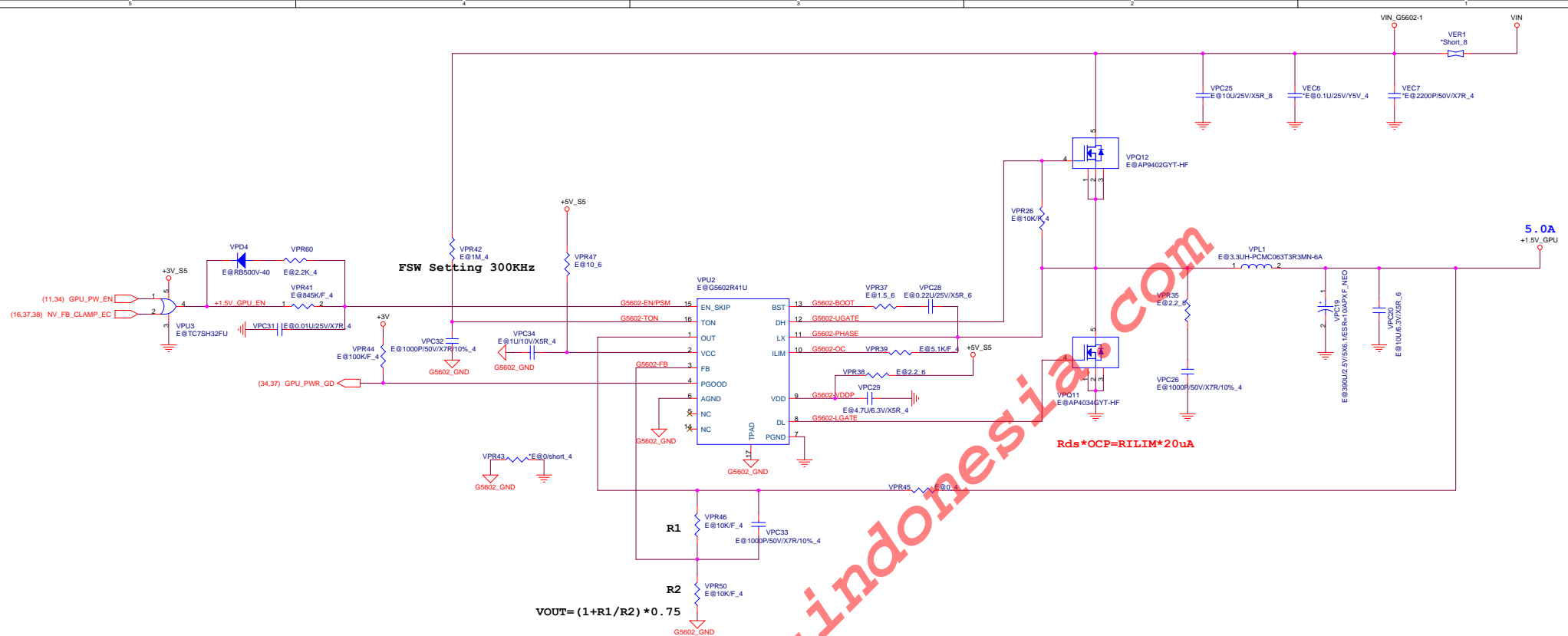
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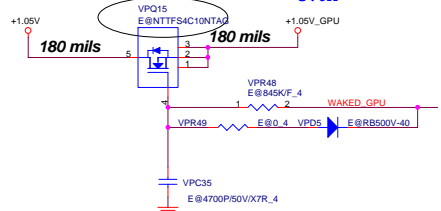
	ACOK	SHDN#	ACID
ADP Normal	1	1	1
ADP UVP	0	0	0



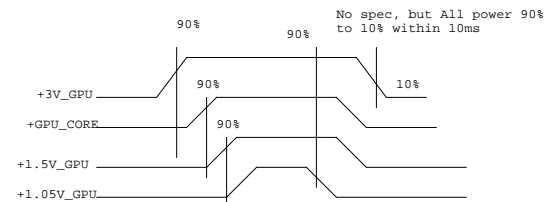
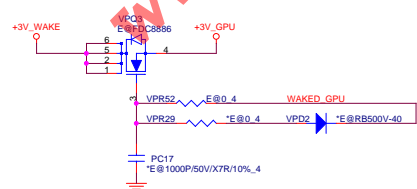


+1.05V_GPU

3.0A



+3V_GPU

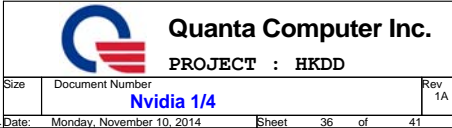


Quanta Computer Inc.
PROJECT : HKDD

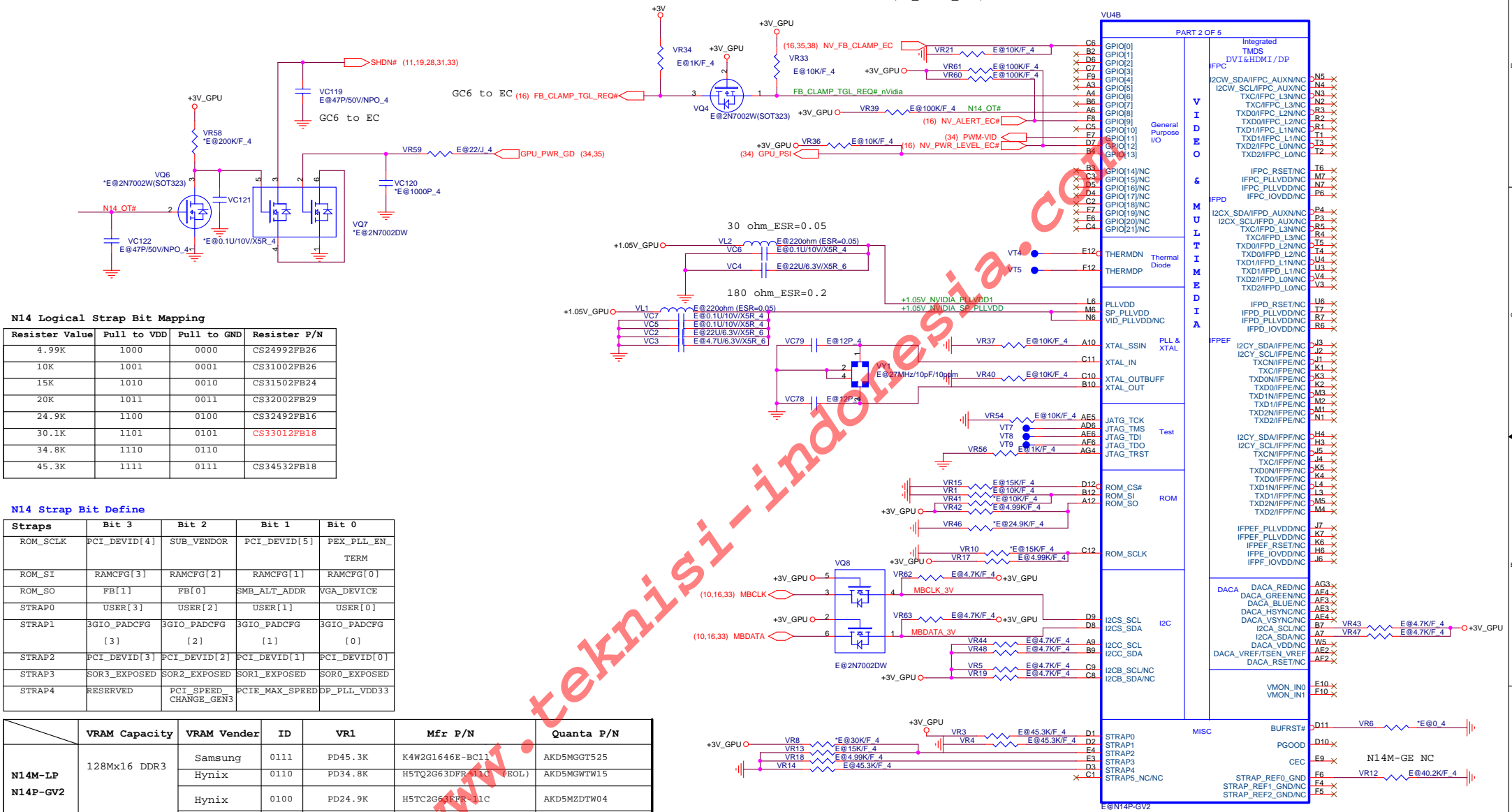
Size	Document Number	Rev
	1.8 GPU / 1.0 GPU	1A

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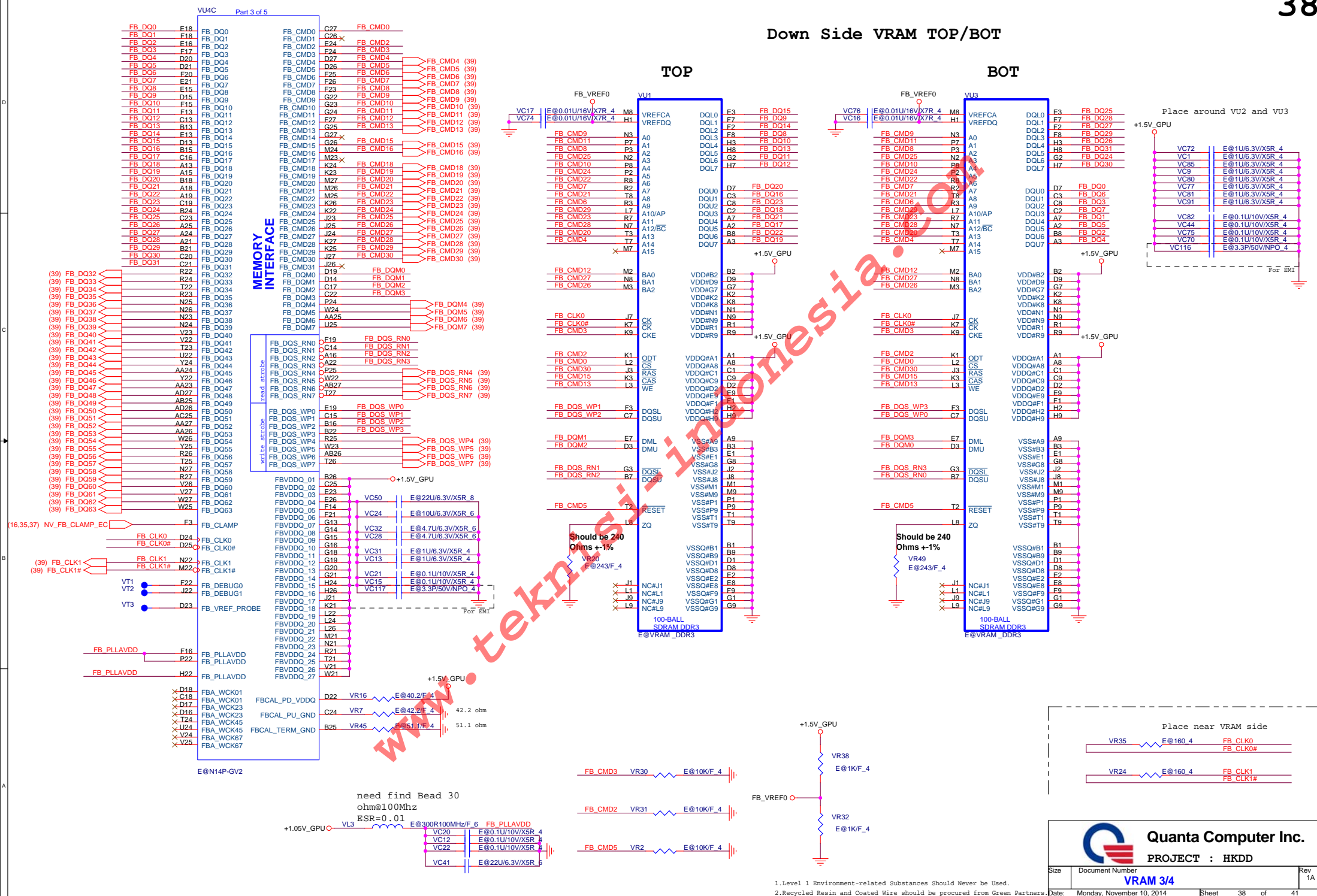
Date: Thursday, November 13, 2014 Sheet 35 of 41



For GC6 GPU Monitor
Status (FB_CLAMP_MON)



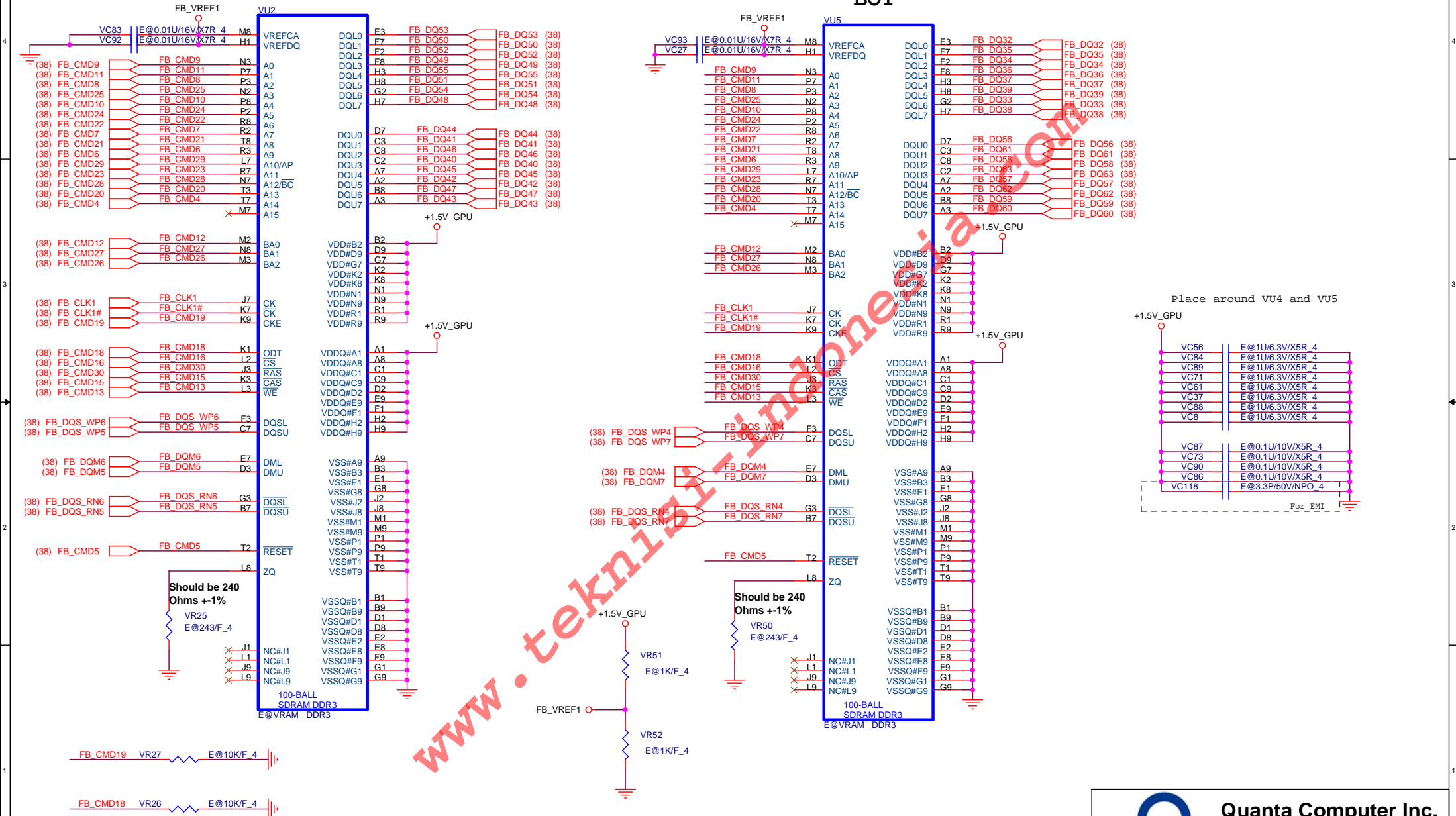
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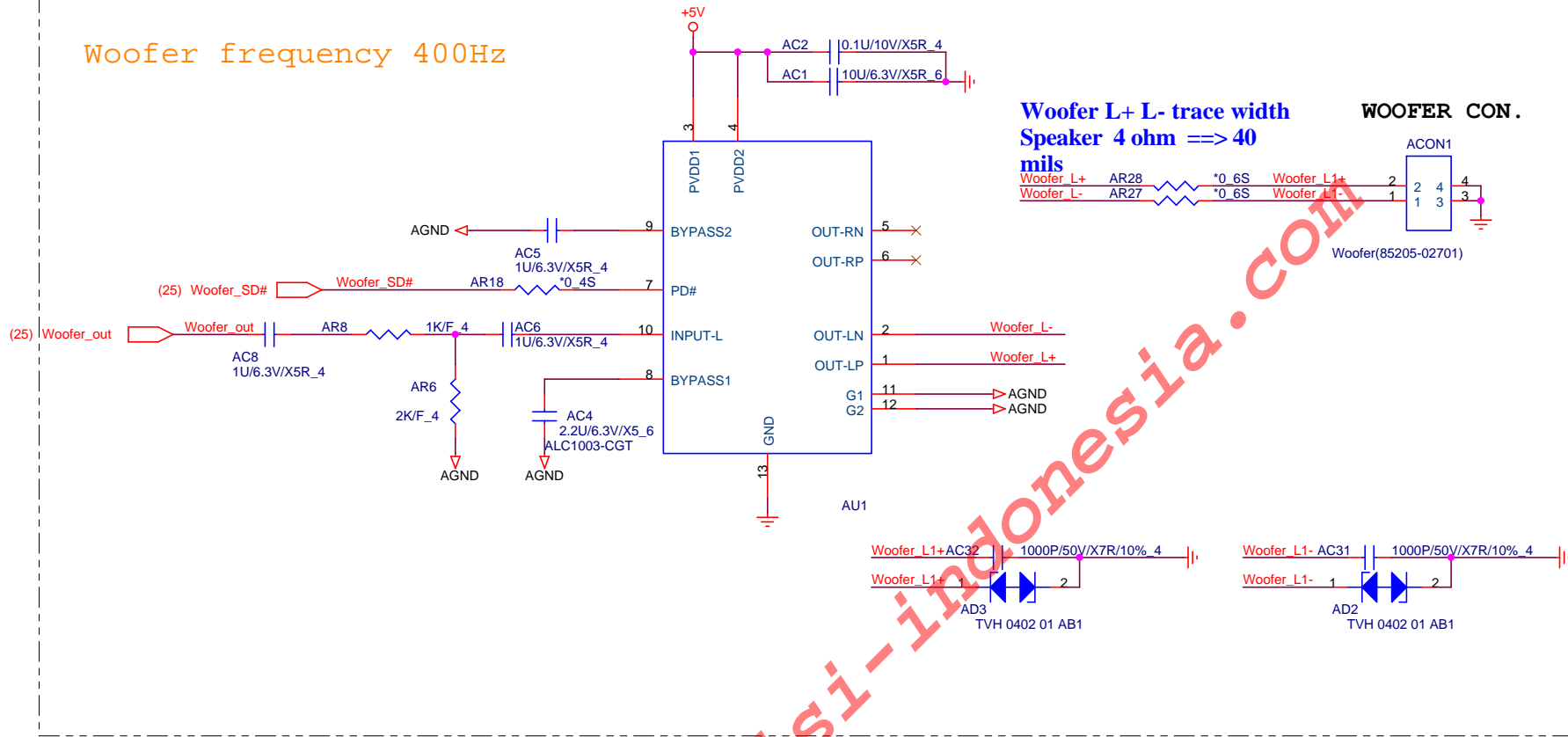
Up Side VRAM TOP/BOT

TOP

BOT

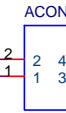


Woofers frequency 400Hz

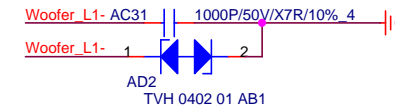
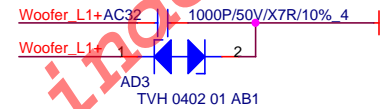


Woofer L+ L- trace width
Speaker 4 ohm ==> 40
mils

WOOFER CON.



Woofer(85205-02701)



Quanta Computer Inc.

PROJECT : HKDD

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		1A
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1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green
Partners.

USB PORT Architecture	
PORT 0	USB3.0
PORT 1	USN3.0
PORT 2	USN2.0
PORT 3	USB2.0
PORT 4	NFC
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A
PORT 9	WiMax/BT
PORT 10	Camera
PORT 11	Card Reader
PORT 12	Touch Screen
PORT 13	N/A

PCIE BUS	
PORT 1	WLAN Port
PORT 2	CARD READER
PORT 3	GLAN (RTL8111G)
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A
PORT 4	ODD
PORT 5	N/A

SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88731CHRTZ	0001 001X	0001 0010	0001 0011	Charger
Nvidia	1001 1110	-	1001 1110	Graphice
LIS331DL	0011 101X	0011 1010	0011 1011	G Sensor

SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
VGP-BPS35A	0001 011X	0001 0110	0001 0111	Battery

SM BUS	SMB_PCH_CLK/SMB_PCH_DAT	WRITE	READ	Function
DIMM Module0	1010 000X	1010 0000	1010 0001	DDRIII
DIMM Module 1	1010 010X	1010 0100	1010 0101	DDRIII
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

Not support "DC only"

OS status	S0	S3	DS3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	DS3	S4 (Win8 off) RTC wake Enable WOLAN Enable	S4 (Win8 off) RTC wake Disable WOLAN Disable	S5 Charge Enable	S5 Charge Disable WoL Disable	S5 WoL Enable
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.675V_DDR_VTT	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+0.85V	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+3V_GPU	H	L	L	L	L	L	L	L
+1.05V_GPU	H	L	L	L	L	L	L	L
+VGPU_CORE	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.35V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC WAKE_ON	H	H	H	H	L	H	L	H
+3V_WAKE	H	H	H	H	L	H	L	H
+5V_WAKE	H	H	H	H	L	H	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	H
+3V_S5_DSW	H	H	H	H	L	L	L	H
+3V_SUS	H	H	L	L	L	L	L	L